ETM50E-05

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Application Manual

Real Time Clock Module

RX8130 CE

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ETM50E Revision History

Rev No.	Date	Page	Description
ETM50E-01	--		--
ETM50E-02	05.Oct.2015		Release
ETM50E-03	10.May.2016	1	Corrected a the block diagram.
		4	Add description to [3.2. Pin Functions].
		9	Corrected a [10.1. Characteristic for the fluctuation of the power supply]
		13	Corrected a [7) Clock output function]
		27	Corrected a [14.7.2. Related register of Battery backup switchover function]
ETM50E-04	20.Sep.2016	3	Updated the Recommended soldering pattern
			Optimization of the text.
ETM50E-05	23.Jan.2018	2	Added terminal processing when output terminal is not used.
		3	Added typical value of external dimensions.
		3	Added recommended soldering pattern.
		6	Corrected Max. value of Hihgh- Level input voltage.
		8	Corrected reset delay time (at recovery form backup).
		9	Corrected access wait time.
		20	Changed 7) TSTP bit related table.
		21	Added timer circuit block diagram
		25	Added alarm circuit block diagram
		27	Added time update circuit block diagram
		30	Corrected table operation stages of voltage detection.
		36	Added comment to wait time.
		37	Added comments related to STOP bit in 3)The setting of the clock and calendar.
		42	Added address circulation table of auto increment function.

Contents

Build-in backup battery charge control function
SERIAL-INTERFACE REAL TIME CLOCK MODULE

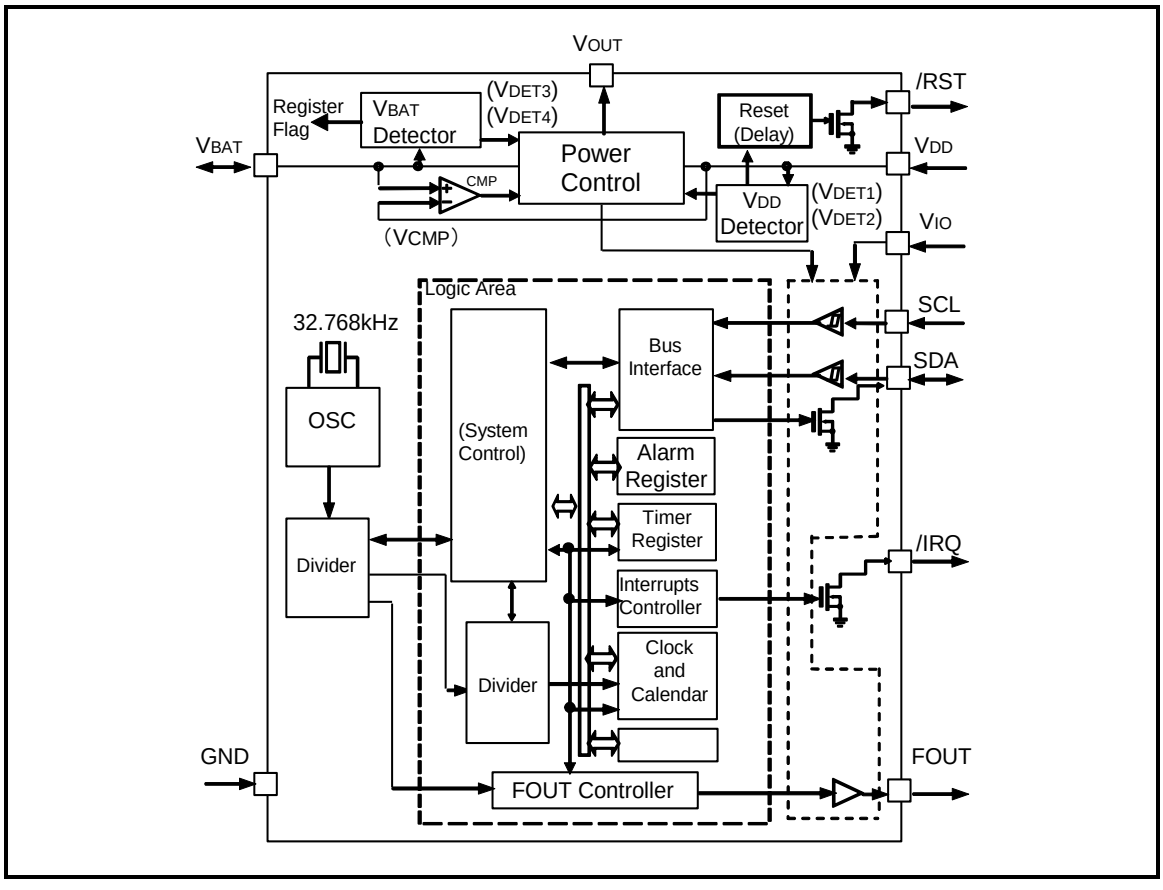
RX8130 CE

- Built in frequency adjusted 32.768 kHz crystal unit.
- Interface type : I²C-Bus interface (up to 400 kHz)
- Wide operating voltage range : 1.6 V to 5.5 V
- Wide timekeeper voltage range : 1.1 V to 5.5 V
- Auto power switching function : Switchover by main power supply monitor.
- Backup battery charge control function : For rechargeable lithium batteries.
- Low leak current : A leak current from a backup power supply pin. 5nA (Max.)
- Reset function : At low supply voltage, external reset signal is generated.
- Low voltage detection : supply voltage and backup voltage detection
- Time correction : digital offset function
- The various function include full calendar, alarm, timer, etc.

1. Overview

This is a real-time clock module of the serial interface system that incorporates a 32.768 kHz crystal oscillator. The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, interval timer, and time update interruption, among other features. By the backup battery charge control function and the interface power supply input pin, RX8130CE can support various power supply circuitries.
All of these many functions are implemented in a thin, compact ceramic package, which makes it suitable for various kinds of small electronic devices.

2. Block Diagram



3. Terminal description

3.1. Terminal connections

RX8130CE

1. VIO
2. SCL
3. SDA
4. FOUT
5. /RST
10. VBAT
9. VOUT
8. VDD
7. GND
6. /IRQ

3.2. Pin Functions

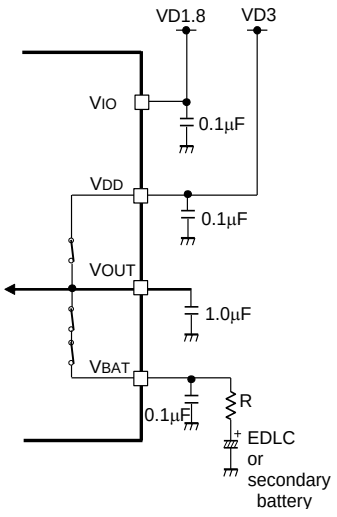
Signal name	I/O	Function
SCL	Input	Serial clock input pin.
SDA	Bi-directional	Data input and output pin.
FOUT	Output	Frequency output pin with output control function. (CMOS) Output frequency can be selected as 32.768kHz, 1024Hz, 1Hz.
/ RST	Open-Drain Output	Even in the backup mode, this pin can opperate. In case of VDD voltage drop detection, a reset signal is outputted. In case of VDD voltage rise detection, it releases the reset signal after 60ms.
/ IRQ	Open-Drain Output	Interrupt output by Alarm and Timer events.(N-ch open drain) This pin can output even a backup mode.
VDD	–	This is a power-supply pin for the internal logic.
VIO	–	This is a interface power supply pin. (There is an level shifter between VDD and VIO)
VOUT	–	Internal voltage output pin. Connect smoothing capacitor of 1.0uF
VBAT	–	This is a power supply pin for backup battery. This is a pin to connect a large-capacity capacitor, a secondary battery, and a primary battery. In a backup mode, the voltage is supplied inside by this pin.
GND	–	Connected to a ground.

Note: Connect a bypass capacitor rated at least 0.1µF between power supply pins and GND pin.
Note: Input pins are able to input up to 5.5V regardless of VIO applied voltage.
Note: Open drain pins are able to Pull-up to 5.5V regardless of VIO applied voltage.
Note: Use the FOUT, /RST, /IRQ terminals as OPEN when not in use.

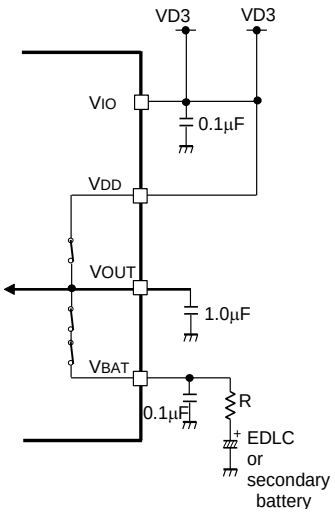
4. Examples of external connection

4.1. Examples of power supply connection

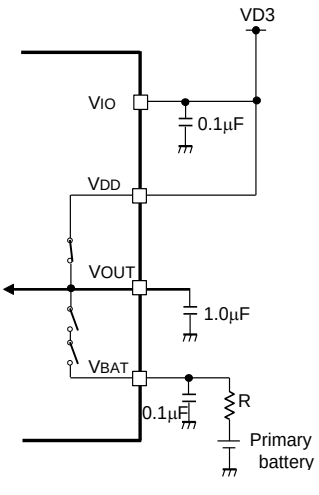
(1) Case of different I/F voltage and charge vlotage



(2) Same I/F voltage and charge voltage (CHGEN=1, INIEN=1)



(3) Primary battery as backup (CHGEN=0)

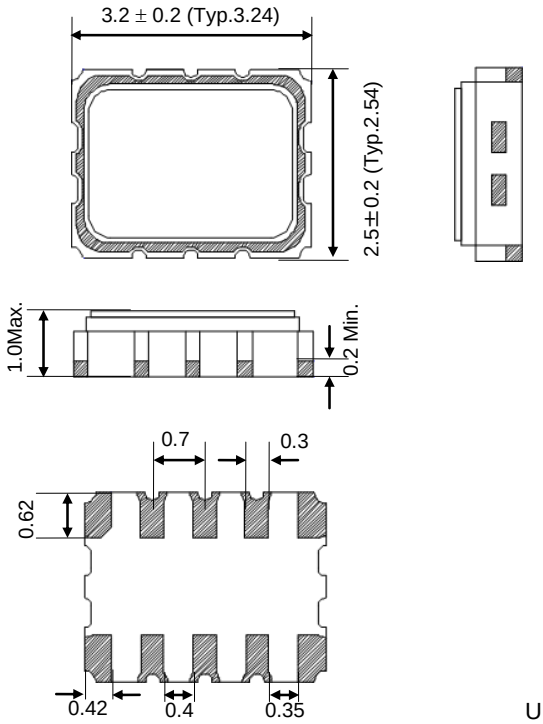


5. External Dimensions / Marking Layout

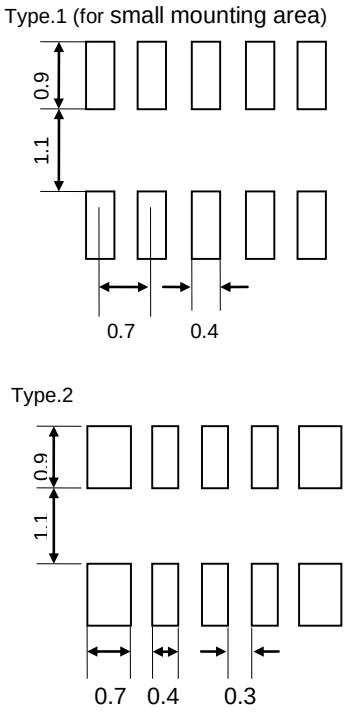
5.1. External Dimensions

RX8130CE

• External dimensions



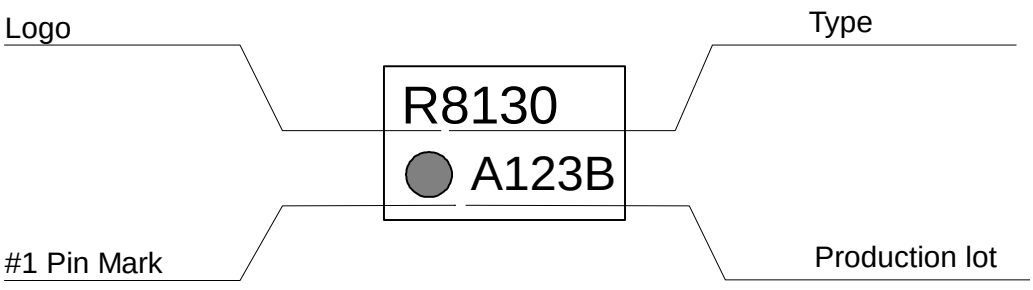
• Recommended soldering pattern



Unit : mm

5.2. Marking Layout

RX8130CE



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

6. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	–	–0.3 ~ +6.5	V
Internal voltage	V_{OUT}	–	–0.3 ~ +6.5	V
Backup supply voltage	V_{BAT}	–	–0.3 ~ +6.5	V
Interface supply voltage	V_{IO}	–	–0.3 ~ +6.5	V
Input voltage 1	V_{IN1}	SCL, SDA	–0.3 ~ +6.5	V
Output voltage 1	V_{OUT1}	/RST, /IRQ, SDA	–0.3 ~ +6.5	V
Output voltage 2	V_{OUT2}	FOUT	-0.3 ~ V_{IO}+0.3	V
Storage temperature	T_{STG}	When stored separately, without packaging	–55 to +125	°C

7. Recommended Operating

*Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Normal operation mode (V_{DD})	1.25	3.0	5.5	V
Interface supply voltage	V_{IO}	V_{DD}=V_{DET1} ~ 5.5V The interface halts when V_{DD} becomes less than V_{DET1}.	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	Backup operation mode (V_{BAT})	1.1	3.0	5.5	V
Operating temperature	$T_{\_use}$	No condensation	–40	+25	+85	°C

∗Minimum value of Clock supply voltage V_{CLK} is the timekeeping continuation lower limit value that initialized RX8130 in operating supply voltage V_{DD}.

8. Frequency Characteristics

*Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output frequency	fo			32.768 (Typ.)		kHz
Frequency stability	Δ f / f	Ta = +25 °C V_{DD} = 3.0 V		5 ± 23 (∗1)		× 10^{-6}
Frequency/voltage characteristics	f / V	Ta = +25 °C V_{DD} = 1.1 V ~ 5.5 V	–2		+2	× 10^{-6} / V
Frequency/temperature characteristics	Top	Ta = –20 °C ~ +70 °C V_{DD} = 3.0 V ; +25 °C reference	–120		+10	× 10^{-6}
Oscillation start time	$t_{\_Str}$	V_{DD} = 2.75 V ~ 5.5 V Internal X'tal oscillation start		0.19	1.0	s
Aging	fa	Ta = +25 °C , V_{BAT} = 3.0 V ; first year	–5		+5	× 10^{-6} / year

∗1) The monthly error is equal to 60 seconds. (excluding offset)

9. Electrical Characteristics

9.1. DC characteristics

*Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

9.1.1. DC characteristics (1)

*Unless otherwise specified, GND = 0 V , V_{BAT}=V_{DD} = 1.1 V ~ 5.5 V , V_{IO}= 1.6 V ~ 5.5 V , Ta = –40°C ~ +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation mode without FOUT (1)	I_{DD}	SCL=SDA = ”H” , FOUT=OFF, /IRQ=OFF, V_{DD}=V_{IO}=3.0V, -40 °C ~ +85 °C CHGEN=0b or V_{BAT}≧V_{DET3}		1500	1600	nA
Current consumption in normal operation with FOUT (2)	I_{32k}	SCL=SDA = ”H” , FOUT=32.768kHz, /IRQ=OFF, V_{DD}=V_{IO}=3.0V, -40 °C ~ +85 °C FOUT pin CL=15pF CHGEN=0b or V_{BAT}≧V_{DET3}		3.5	4.0	uA
Current consumption in backup mode(3)	I_{BAT}	SCL=SDA = ”L” , V_{BAT}=3.0V ,VDD=VIO=0.0V, -40 °C ~ +85 °C		300	500	nA
Detector Threshold Voltage1 (rising edge of V_{DD})	+V_{DET11}	2.75V setting Reset-releases	2.72	2.80	2.88	V
Detector Threshold Voltage1 (falling edge of V_{DD})	-V_{DET11}	2.75V setting、Reset output	2.67	2.75	2.83	V
Detector Threshold Voltage2 (rising edge of V_{DD})	+V_{DET12}	2.7V setting Reset-releases	2.67	2.75	2.83	V
Detector Threshold Voltage2 (falling edge of V_{DD})	-V_{DET12}	2.7V setting , Reset output	2.62	2.70	2.78	V
Detector Threshold Voltage3 (rising edge of V_{DD})	+V_{DET2}	Switching voltage from V_{BAT} to V_{DD}	1.25	1.35	1.45	V
Detector Threshold Voltage3 (falling edge of V_{DD})	-V_{DET2}	Switching voltage from V_{DD} to V_{BAT}	1.20	1.30	1.40	V
Detector Threshold Voltage1 (rising edge of V_{BAT})	+V_{DET31}	Charge stop voltage (full charge) BFVSEL=00b	2.94	3.02	3.10	V
Detector Threshold Voltage1 (falling edge of V_{BAT})	-V_{DET31}	Recharge voltage. BFVSEL=00b	2.89	2.97	3.05	V
Detector Threshold Voltage2 (rising edge of V_{BAT})	+V_{DET30}	Charge stop voltage (full charge) BFVSEL=10b	2.84	2.92	3.00	V
Detector Threshold Voltage2 (falling edge of V_{BAT})	-V_{DET30}	Recharge voltage. BFVSEL=10b	2.79	2.87	2.95	V
Detector Threshold Voltage3 (rising edge of V_{BAT})	+V_{DET32}	Charge stop voltage (full charge) BFVSEL=01b	3.00	3.08	3.16	V
Detector Threshold Voltage3 (falling edge of V_{BAT})	-V_{DET32}	Recharge voltage. BFVSEL=01b	2.95	3.03	3.11	V
V_{BAT} end voltage	-V_{DET4}	Low VBATdetection Register flag VBLF = 1b	2.32	2.40	2.48	V
V_{DD}-V_{OUT} off-leak current	I_{SW1}	V_{OUT}=3.0V、V_{DD}=0.0V			5.0	nA
V_{BAT}-V_{OUT} off-leak current	I_{SW2}	V_{BAT}=3.0V、V_{OUT}=0.0V			5.0	nA

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
V_{OUT} output voltage 1	V_{VOUT1}	V_{DD}=3.0V、I_{OUT}=1mA			V_{DD}-0.06		V
V_{OUT} output voltage 2	V_{VOUT2}	V_{BAT}=3.0V、I_{OUT}=0.1mA			V_{BAT}-0.02		V
High-level input voltage	V_{IH1}	SCL, SDA		0.8 × V_{IO}		5.5	V
Low-level input voltage	V_{IL}	SCL, SDA		GND – 0.3		0.2 × V_{IO}	V
High-level output voltage	V_{OH}	FOUT	I_{OH}=-1 mA	V_{IO}–0.5		V_{IO}	V
Low-level output voltage	V_{OL1}	FOUT	I_{OL}=1 mA	GND		GND+0.5	V
	V_{OL2}	/RST,/IRQ	V_{IO}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
	V_{OL3}		V_{IO}=3 V, I_{OL}=1 mA	GND		GND+0.4	V
	V_{OL4}	SDA	V_{IO} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V

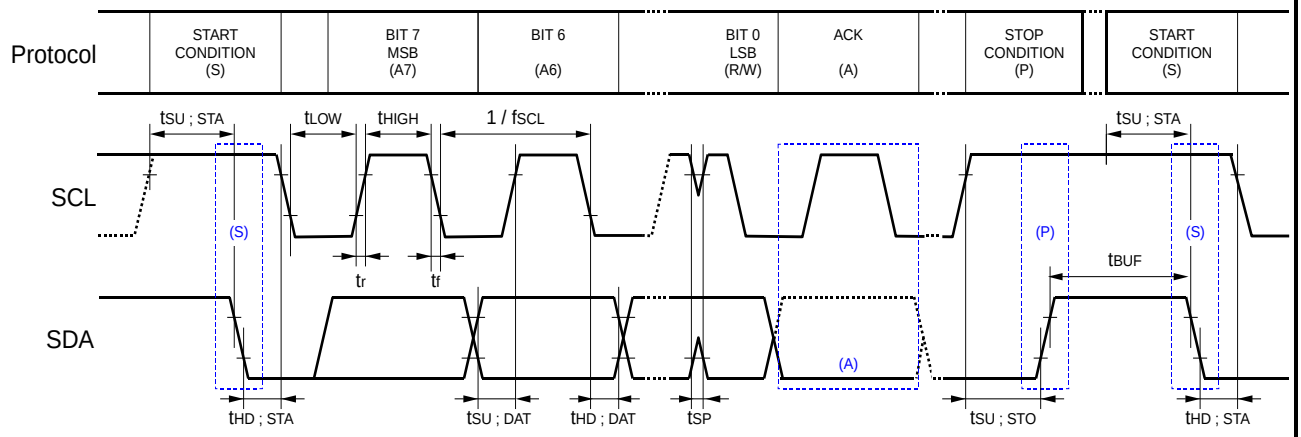
9.2. AC characteristics

9.2.1. AC characteristics(1)

*Unless otherwise specified, GND = 0 V , V_{IO}= 1.6 V ~ 5.5 V , Ta = –40°C ~ +85°C

Item	Symbol	Standard-Mode (f_{SCL}=100kHz)		Fast-Mode (f_{SCL}=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Start condition setup time	$t_{SU;STA}$	4.7		0.6		µs
Start condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		ns
Stop condition setup time	$t_{SU;STO}$	4.0		0.6		µs
Bus idle time between start condition and stop condition	t_{BUF}	4.7		1.3		µs
Time when SCL = "L"	t_{LOW}	4.7		1.3		µs
Time when SCL = "H"	t_{HIGH}	4.0		0.6		µs
Rise time for SCL and SDA	t_r		1.0		0.3	µs
Fall time for SCL and SDA	t_f		0.3		0.3	µs
Allowable spike time on bus	t_{SP}		50		50	ns

- Timing chart



Warning: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 0.95 seconds**.
If such communication requires **0.95 seconds** or longer, the I^2C bus interface is reset by the internal bus timeout function.
When bus-time-out occur, SDA turns to Hi-Z input mode.

Note:During access to the time registers, the time counting is on hold! This means that up to 1 second can be “lost” in case of unsuccessful communication as mentioned above!
Please make sure to send I2C start condition before actual transmission of the RTCs slave address as otherwise the slave address appears to be shifted by 1 bit!

9.2.2. AC characteristics(2)

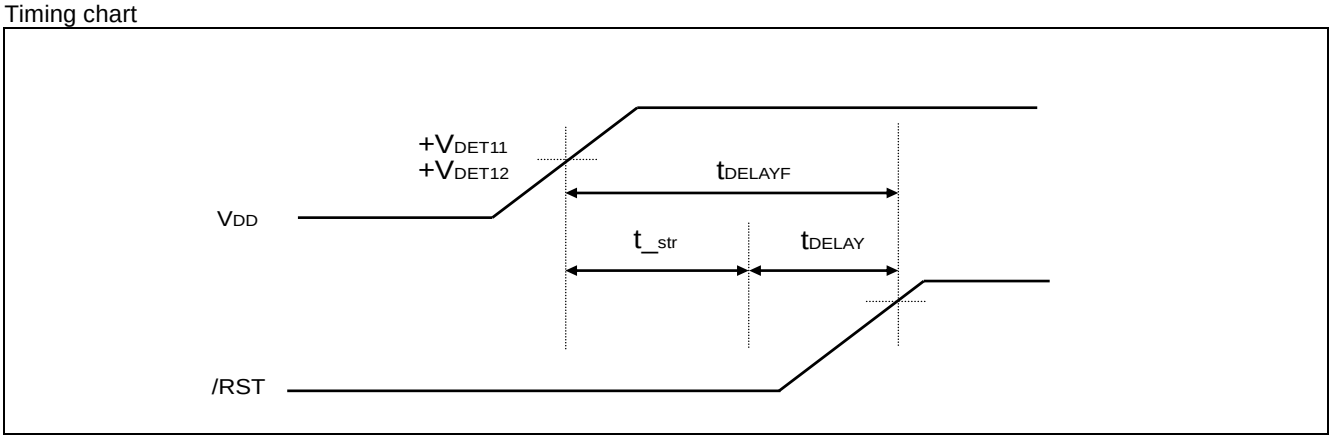
※Unless otherwise specified、GND=0 V , V_{IO}=1.6 V ~ 5.5 V , Ta= –40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT symmetry	SYM	50% V_{IO} Level	40		60	%

9.2.3. AC characteristics(3)

Item	symbol	Min	Typ	Max	unit
Reset internal delay time	t_{DELAY}		60		ms
Reset delay time (Initial power ON)	t_{DELAYF}		250 (t_str+t_{DELAY})		ms

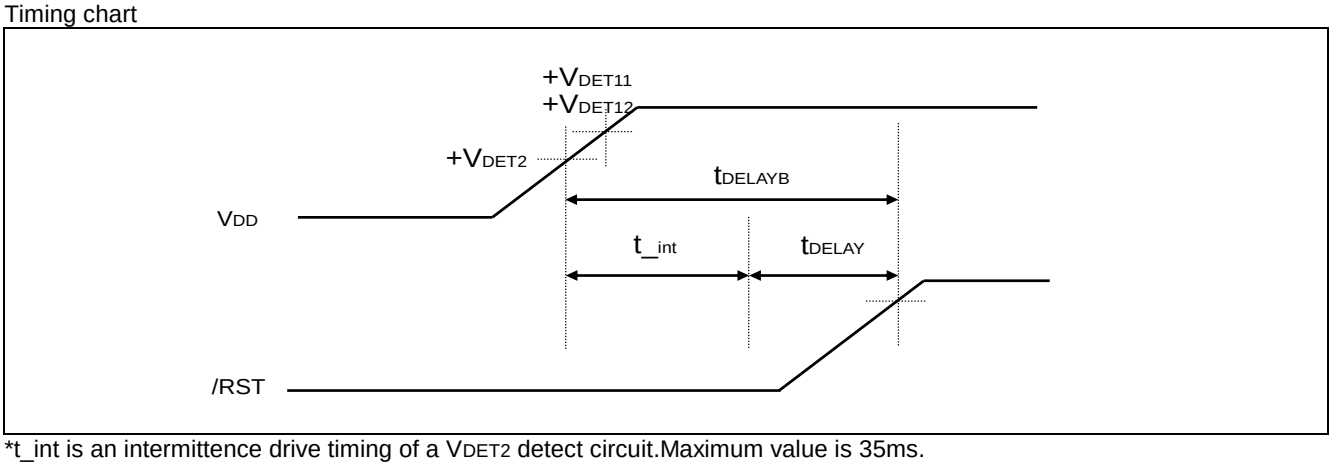
Timing chart



* t_str is oscillation startup time.

Item	symbol	Min	Typ	Max	unit
Reset delay time (Recovery from Backup) t_int+t_DELAY	t_{DELAYB}	60		95	ms

Timing chart

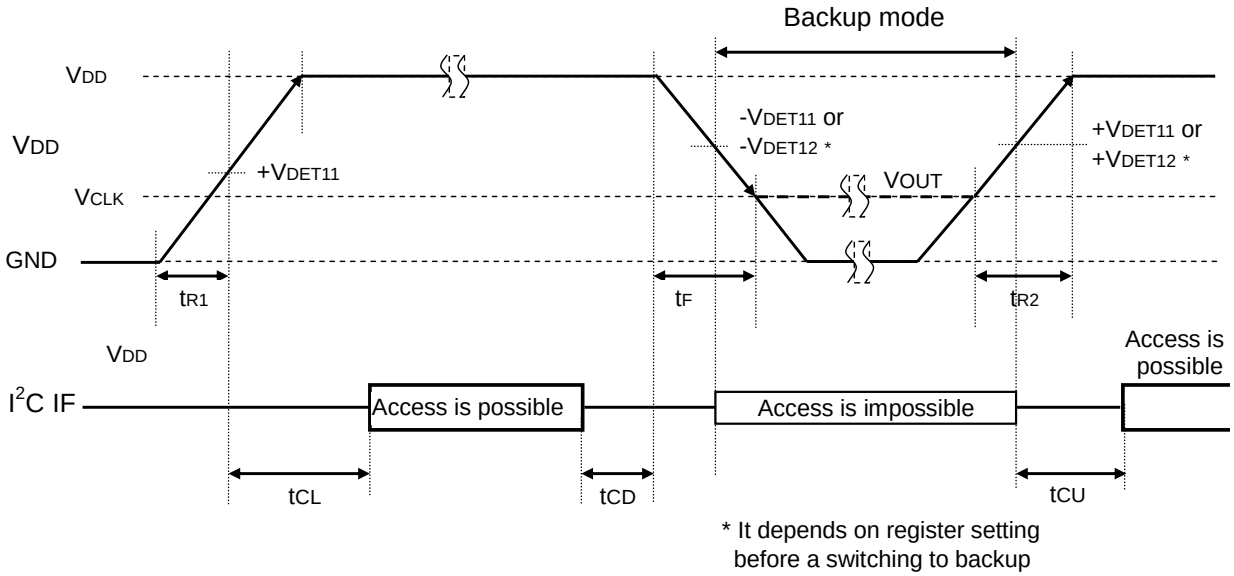


*t_int is an intermittence drive timing of a V_{DET2} detect circuit.Maximum value is 35ms.

10. Matters that demand special attention on use

10.1. Characteristic for the fluctuation of the power supply

*This circuit is sensitive to power supply noise and supply voltage should be stabilized to avoid negative impact on the accuracy.
* tR1 is needed for a proper power-on reset. If this power-on condition can not be kept, it is necessary to send a initialization routine to the RTCby software.
*In case of repeated ON/OFF of the power supply within short term, it is possible that the power-on reset becomes unstable.
After power-OFF, keep VDD=VBAT=GND for more than 10 seconds for a proper power-on reset.
When it is impossible, please initialize the RTC by the software.
* Before shifting to a backup operation, please transfer stop condition and finish communication as otherwise data might be lost or a time error of 1sec might occur.



* It depends on register setting before a switching to backup

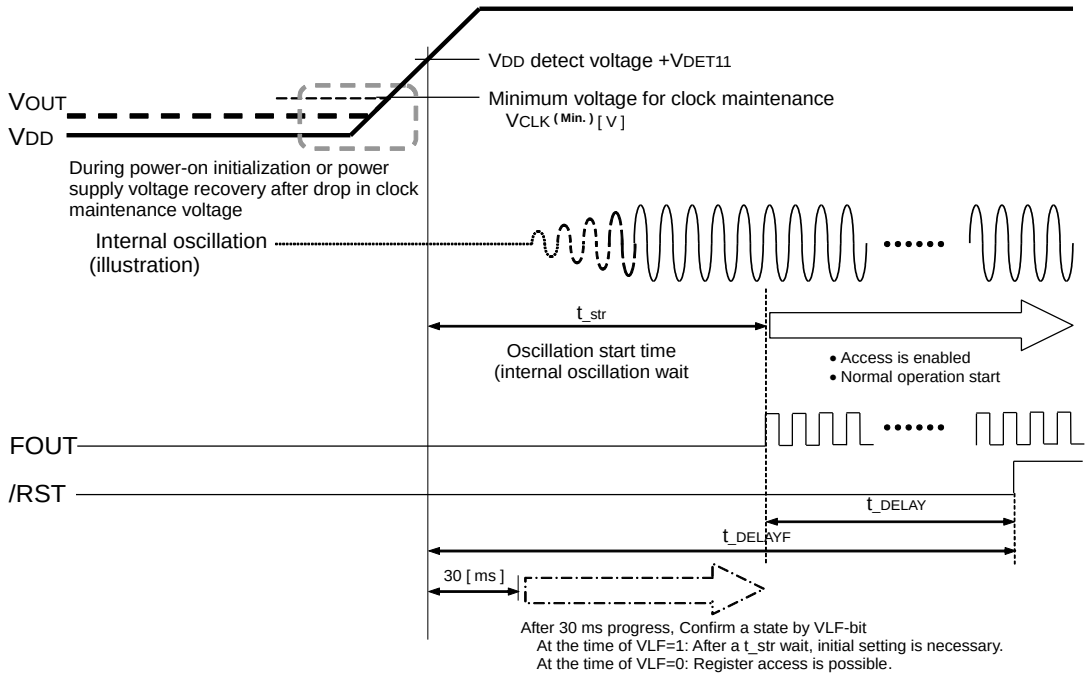
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	t_{R1}	From GND to V_{DD}=+V_{DET11}	0.1	-	10	ms / V
access wait time (Initial power on)	t_{CL}	After arrival to V_{DD}=+V_{DET11}	30	-	-	ms
Backup switchover start wait time	t_{CD}	After the access end	0	-	-	ms
Power supply fall time	t_F	From V_{DD} toV_{DD}=-VDET1x	1	-	-	ms / V
Power supply rise time (Recovery from Backup)	t_{R2}	Recovery to the operating voltage	1	-	-	ms / V
Access wait time (Recovery from Backup)	t_{CU}	After arrival to V_{DD}=+V_{DET1x}	35	-	-	ms

10.2. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup

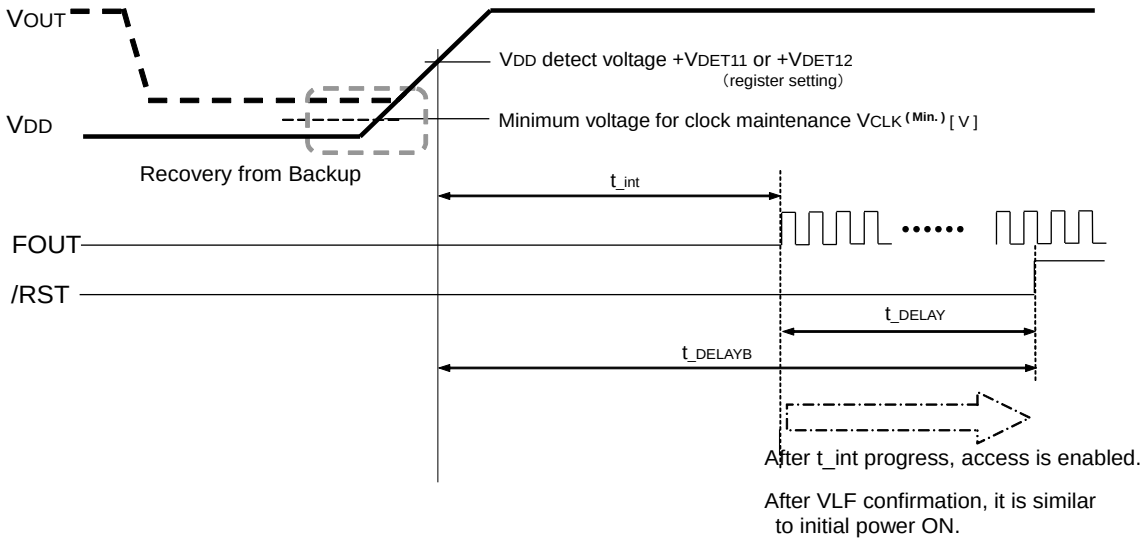
•

Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized. Please initialize the RTCat the time thepower supply voltage returns (VLF = 1) after the oscillation has stabilized (after oscillation start time tSTA).

If intending to access the RTC after the main supply voltage returns, please note following points:



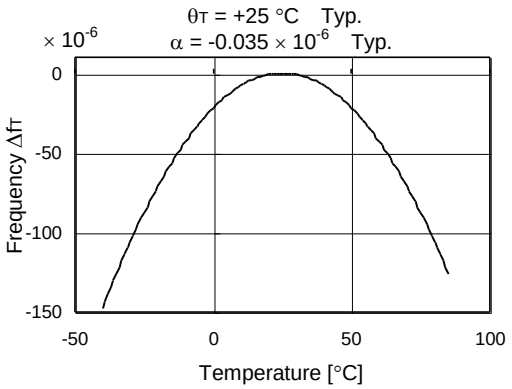
- Recovery from Backup



11. Reference information

11.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
   - θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/fo + \Delta f_T + \Delta fv$

   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/fo$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δfv : Frequency deviation in any voltage.

3. How to find the date difference

   Date Difference = $\Delta f/f \times$ 86400(Sec)

   ∗ For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

12. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electronic noise near this module.

(3) Voltage levels of input pins

When the voltage of out of the input voltage specifications range input into an input terminal constantly, a penetration electric current occurs. Thus, current consumption increases very much. This causes Latch-up, and there is the case that, as a result, a built-in IC is destroyed. Please use an input terminal according to input voltage specifications.
Furthermore, please input the V_{IO} or GND most recent voltage as much as possible.

(4) Handling of unused pins

Disposal of unused input terminals. When an input terminal is open state, it causes increase of a consumption electric current and the behavior that are instability. Please fix an unused input terminal to the voltage that is near to V_{IO} or GND.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

(6) Installation of charged battery.

When a charged backup battery is installed by soldering, battery connection terminal of this device should connect to GND, beforehand.

13. Overview of Functions and Description of Registers

Note:
The initialization of the register is necessary about the unused function.

13.1. Overview of Functions

1) Clock functions

This function is used to set and read out second, minute, hour, day, month, year (to the last two digits), and date data.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.
At the start of a I2C communication, the time and clock counting stops (which causes loss of time), and clock starts automatically again at the end of the I2C communication.

2) Fixed-cycle Timer Interrupt function

The fixed-cycle timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 65535 hours.
When an interrupt event is generated, the /IRQ pin goes to low level ("L") and "1" is set to the TF bit to report that an event has occurred.

3) Long-Timer function

It is able to use fixed cycle timer interrupt function as Long-Timer or usage counter.
This function measures the operation time on the main power supply and the operation time on the backup power supply and can automatically sum them up.

4) Alarm interrupt function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.

5) Time Update Interrupt Function

The time update interrupt function generates interrupt in one-second or one-minute intervals which are synchronized to the update of the second or minute time register of the RTC When an interrupt event is generated, the /IRQ pin goes to low level ("L") and "1" is set to the UF bit to report that an event has occurred.

6) Frequency stop detection function

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss might have occured due to a low supply voltage.

7) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin. Output could also be 1Hz, or 1024Hz.

8) User RAM

RAM register is read/write accessible for any data.

9) Digital offset function

The clock precision can be increased by adding a time offset.

13.2. Register table

13.2.1. Register table

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	○	40	20	10	8	4	2	1
11	MIN	○	40	20	10	8	4	2	1
12	HOUR	○	○	20	10	8	4	2	1
13	WEEK	○	6	5	4	3	2	1	0
14	DAY	○	○	20	10	8	4	2	1
15	MONTH	○	○	○	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	MIN Alarm	AE	40	20	10	8	4	2	1
18	HOUR Alarm	AE	•	20	10	8	4	2	1
19	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	TSEL2	TSEL1	TSEL0
1D	Flag Register	VBLF	o	UF	TF	AF	RSF	VLF	VBFF
1E	Control Register0	***TEST***	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE
1F	Control Register1	SMP TSEL1	SMP TSEL0	CHG EN	INIEN	o	RS VSEL	BF VSEL1	BF VSEL0

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20 | 23	RAM	User Register 32 bit (4 word x 8 bit)							

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1

∗1. After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗2. The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing. ∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing

∗3. Any bit marked with "○" should be used with a value of "0" after initialization

∗4. Any bit marked with "•" is a RAM bit that can be used to read or write any data.

∗5. User Register is a free register which can be used as user RAM.

∗6. The above table shows only the user registers. Due to functional reasons, RTC has different registers not mentioned above table which are programmed by the manufactorer. Please make sure to only access above mentioned user registers.

13.2.2. Register initial value , and Read/Write operation table

【 0: Write impossible、Read value "0" Fix 】
【 X: Undefined (Initialization by register writing is needed)】
【 **0**: Reset state 】
【 **1**: Set state 】

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	X	X	X	X	X	X	X
11	MIN	0	X	X	X	X	X	X	X
12	HOUR	0	0	X	X	X	X	X	X
13	WEEK	0	X	X	X	X	X	X	X
14	DAY	0	0	X	X	X	X	X	X
15	MONTH	0	0	0	X	X	X	X	X
16	YEAR	X	X	X	X	X	X	X	X
17	MIN Alarm	X	X	X	X	X	X	X	X
18	HOUR Alarm	X	X	X	X	X	X	X	X
19	WEEK Alarm	X	X	X	X	X	X	X	X
	DAY Alarm		X	X	X	X	X	X	X
1A	Timer Counter 0	X	X	X	X	X	X	X	X
1B	Timer Counter 1	X	X	X	X	X	X	X	X
1C	Extension Register	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
1D	Flag Register	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
1E	Control Register0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1F	Control Register1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20-23	RAM	X	X	X	X	X	X	X	X

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

13.3. Description of registers

13.3.1. Clock and calender counter (10[h] ~ 16[h])

This is counter registers from a second to a year.

∗ Please refer to [14.1 Clock calendar explanation] for details.

13.3.2. RAM registers (20[h] ~ 23[h])

This RAM register is read/write accessible for any data in the range from 00 h to FF h.

13.3.3. Alarm registers (17[h] ~ 19[h])

The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.

∗ Please refer to [14.3. Alarm Interrupt Function] for the details.

13.3.4. Timer setting and Timer counter register (1A[h] ~ 1E[h])

This register is used to set the default (preset) value for the counter.

To use the fixed-cycle timer interrupt function,TE, TF, TIE, TSEL2,TSEL1, TSEL0,TBKON,TBKE bits are set and used. When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits. ∗ Please refer to [14.2. Fixed-cycle Timer Interrupt Function] for the details.

13.3.5. Function-related register 1 (1C[h] ~ 1E[h])

1) FSEL1, FSEL0 bit

A combination of the FSEL1 and FSEL0 bits are used to select the frequency to be output.
The choice is possible by a combining FSEL-bits and CE/FOE-pin, select the frequency of clock output or inhibit the clock output. ∗ Please refer to [14.6. FOUT Function] for the details.

2) USEL , UF, UIE bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.
∗ Please refer to [14.4. Update interrupt function] for the details.

3) TE, TF, TIE, TSEL2, TSEL1, TSEL0, TSTP,TBKON,TBKE bit

These bits are used to control operation of the fixed-cycle timer interrupt function.

4) WADA, AF, AIE bit

These bits are used to control operation of the alarm interrupt function.

5) ***TEST*** bit

These bits are the manufacturer's test bit. Always leave this bit value as "0" ..

6) VLF bit

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop.
∗ Please refer to [14.5. Frequency stop detection function] for the details.

7) STOP bit

This bit is to stop a timekeeping operation. In the case of “STOP bit = 1":

∗ 1) All the update of timekeeping and the calendar operation stops.
With it, an update interrupt event does not occur at an alarm interrupt and the time.

∗ 2) The part of the fixed-cycle timer interrupt function stops.
A count stops the source clock setting of the timer in case of "64Hz, 1Hz, 1min, 1h".

∗ 3) Note 3: The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz and 1024Hz output is possible. But 1Hz output is disabled.

∗ 4) Switchover function cannot work in order that the V_{DD} voltage drop detection stops even if a main power supply falls.

8) RSF bit

This flag bit holds the result of detecting the reset voltage.

13.3.6. Function-related register 2 (1F[h])

1) SMPTSEL1,SMPTSEL0 bit

Operation time setting of a voltage detector circuit for each power supply pin.
∗ Please refer to [14.7. Battery Backup switchover function] for the details.

2) CHGEN bit

Setting of backup battery charge control (ON/OFF).

3) INIEN bit

Setting of a power switchover function (ON/OFF).

4) RSVSEL bit

Setting of voltage detection level of a V_{DD} pin.

5) BFVSEL1,BFVSEL0 bit

Setting of the full charge detection voltage of a backup battery.

13.3.7. Digital offset register (30[h])

1) DTE bit

Setting of a Digital offset function (ON/OFF).
∗ Please refer to [14.10. Digital offset function] for the details.

2) L7 ~ L1 bit

Setting of a Digital offset value.

14. How to use

14.1. Clock calendar explanation

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end. Therefore it recommends that the access to a clock calendar has continuous access by the auto increment function.

Setting example: Sun, 29-Feb-88 17:39:45 (leap year)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	1	0	0	0	1	0	1
11	MIN	0	0	1	1	1	0	0	1
12	HOUR	0	0	0	1	0	1	1	1
13	WEEK	0	0	0	0	0	0	0	1
14	DAY	0	0	1	0	1	0	0	1
15	MONTH	0	0	0	0	0	0	1	0
16	YEAR	1	0	0	0	1	0	0	0

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

14.1.1. Clock counter

1) [SEC] [MIN] register

These registers are 60-base BCD counters. These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.
When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512Hz ~ 1 Hz) is cleared to 0.

2) [HOUR] register

This register is a 24-base BCD counter (24 hour format).These registers are incremented at the timing when carry is generated from a lower register.

14.1.2. Week counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.

The setting example of the week register value.

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data [h]
Sunday	0	0	0	0	0	0	0	**1**	01 h
Monday	0	0	0	0	0	0	**1**	0	02 h
Tuesday	0	0	0	0	0	**1**	0	0	04 h
Wednesday	0	0	0	0	**1**	0	0	0	08 h
Thursday	0	0	0	**1**	0	0	0	0	10 h
Friday	0	0	**1**	0	0	0	0	0	20 h
Saturday	0	**1**	0	0	0	0	0	0	40 h

∗ Do not set "1" to more than one day at the same time.

14.1.3. Calendar counter

1) [DAY], [MONTH] resister

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is 12-base BCD counter. when carry is generated from a lower register.

		Jan.	Feb.	Mar	Apr.	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Days	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

2) [YEAR] register

This register is a BCD counter for years 00 to 99.
The leap year is automatically determined, which reflects in the DAY register.

14.2. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 65535 hours. This function can stop at one time and is available as a accumulative timer. After the interrupt occurs, the /IRQ status is automatically cleared .

14.2.2. Related registers for function of fixed-cycle timer interrupt function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Extension Register	FSEL1	FSEL0	USEL	**TE**	WADA	**TSEL2**	**TSEL1**	**TSEL0**
1D	Flag Register	VBLF	o	UF	**TF**	AF	RSF	VLF	VBFF
1E	Control Register0	***TEST***	STOP	UIE	**TIE**	AIE	**TSTP**	**TBKON**	**TBKE**

∗ Before entering operation settings, we recommend first clearing the TE bit to "0" .
∗ When the fixed-cycle timer function is not being used, the fixed-cycle Timer Counter0,1 register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) Down counter for fixed-cycle timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 (0001 h) to 65535 (FFFFh) can be set.
Be sure to write "0" to the TE bit before writing the preset value.

∗ When TE=0, read out data of timer counter is default (Preset) value.And when TE=1, read out data of timer counter is just counting value.But, when access to timer counter data, counting value is not held. Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is necessary.

2) TSEL2, TSEL1, TESL0 bit

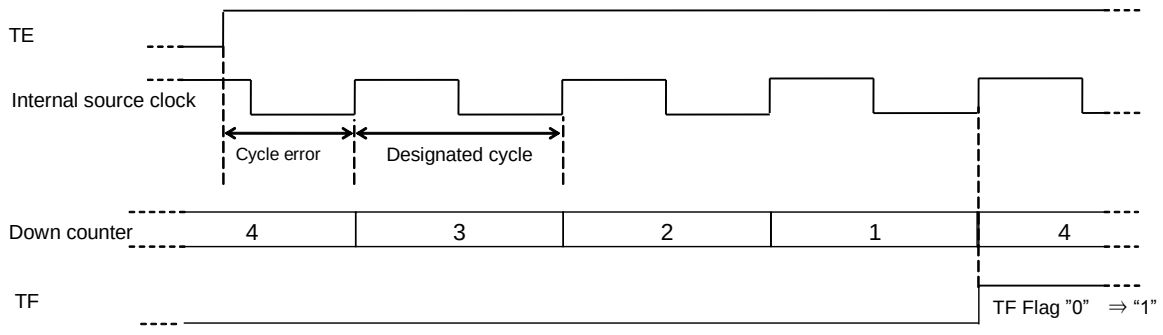
The combination of these three bits is used to set the countdown period (source clock) for this function.

TSEL2 (bit 2)	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN (min)
0	0	0	4096 Hz /Once per 244.14 μs	122 μs
0	0	1	64 Hz /Once per 15.625 ms	7.57 ms
0	1	0	1 Hz /Once per second	7.57 ms
0	1	1	1/60 Hz /Once per minute	7.57 ms
1	0	0	1/3600 Hz /Once per hour	7.57 ms

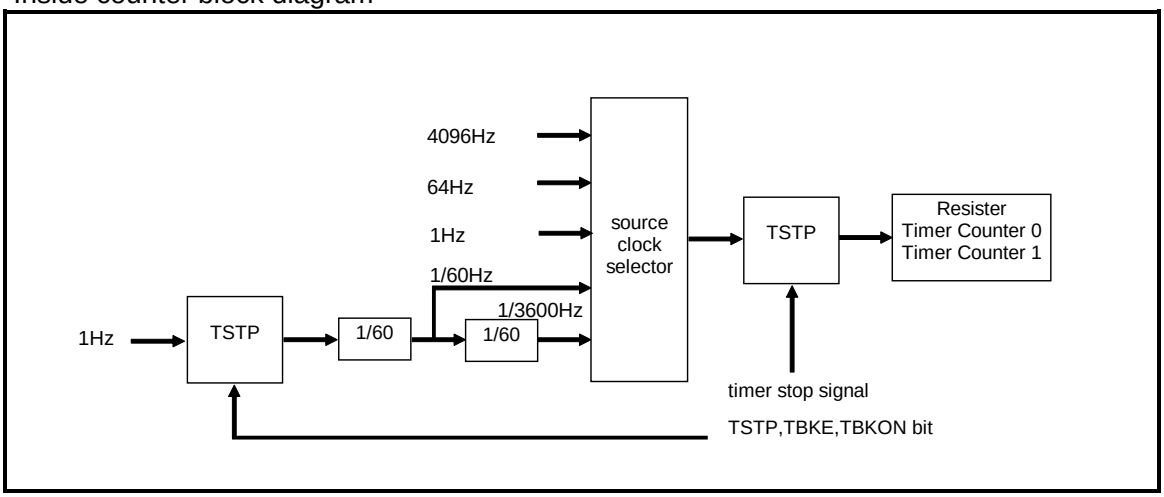
∗1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) The first countdown shortens than a source clock.
When selected 4,096Hz / 64HZ / 1Hz as a source clock, one period of error occurs at the maximum.
When selected1/60Hz / 1/3600Hz as a source clock, 1Hz of error occurs at the maximum.

The example of the error of the first countdown: A value to preset is 0004h



Inside counter block diagram



∗ The resolution of the count value depends on the source clock

3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write	0	Stops fixed-cycle timer interrupt function. ∗ Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	Starts fixed-cycle timer interrupt function. ∗ The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	–
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a fixed-cycle timer interrupt event has occurred.

TIE	Data	Description
Write	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated. 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

6) TBKON, TBKE bit

This function selects the operation time with the main power supply or the operation time with the backup power supply. The count value is added.

operation	**TBKE**	**TBKON**	Description
Write	0	X	This setting counts normal mode and backup mode.
	1	0	This setting counts it at time of normal mode(V_{DD} operation)
		1	This setting counts it at time of backup mode (V_{BAT} operation)

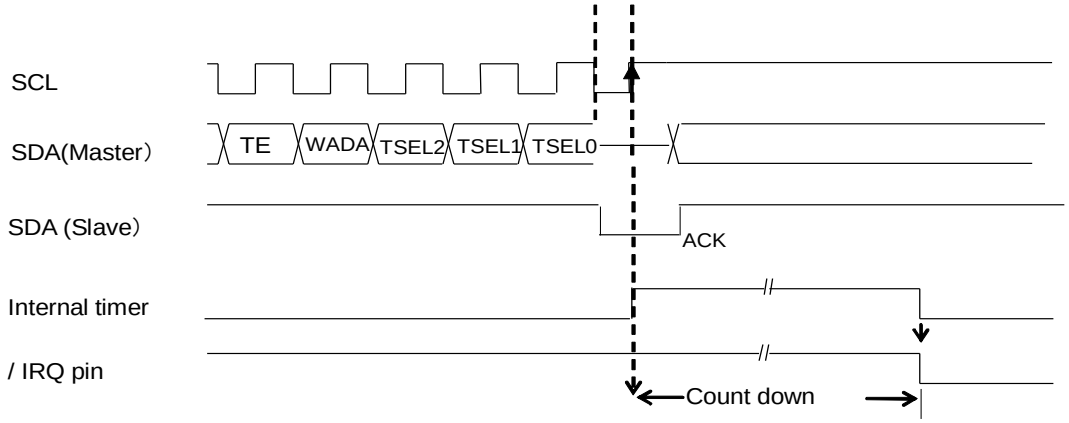
7) TSTP bit (Timer Stop)

This bit is used to stop fixed-cycle timer count down.

TE	STOP	TBKE	TSTP	Description
1	0	0	0	Writing a "0" to this bit cancels stop status (restarts timer count down). ∗The reopening value of the countdown is a stopping value
			1	Count stops.
		1	X	Setting of TSTP value becomes invalid, and the count does not stop even if set it in TSTP="1".
	1	X	X	The count stops at the time of the setting of 64Hz, 1Hz,1/60Hz,1/3600Hz.
0	X	X	X	It doesn't start counting

14.2.3. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL (ACK output) signal that occurs when the TE value is changed from "0" to "1".

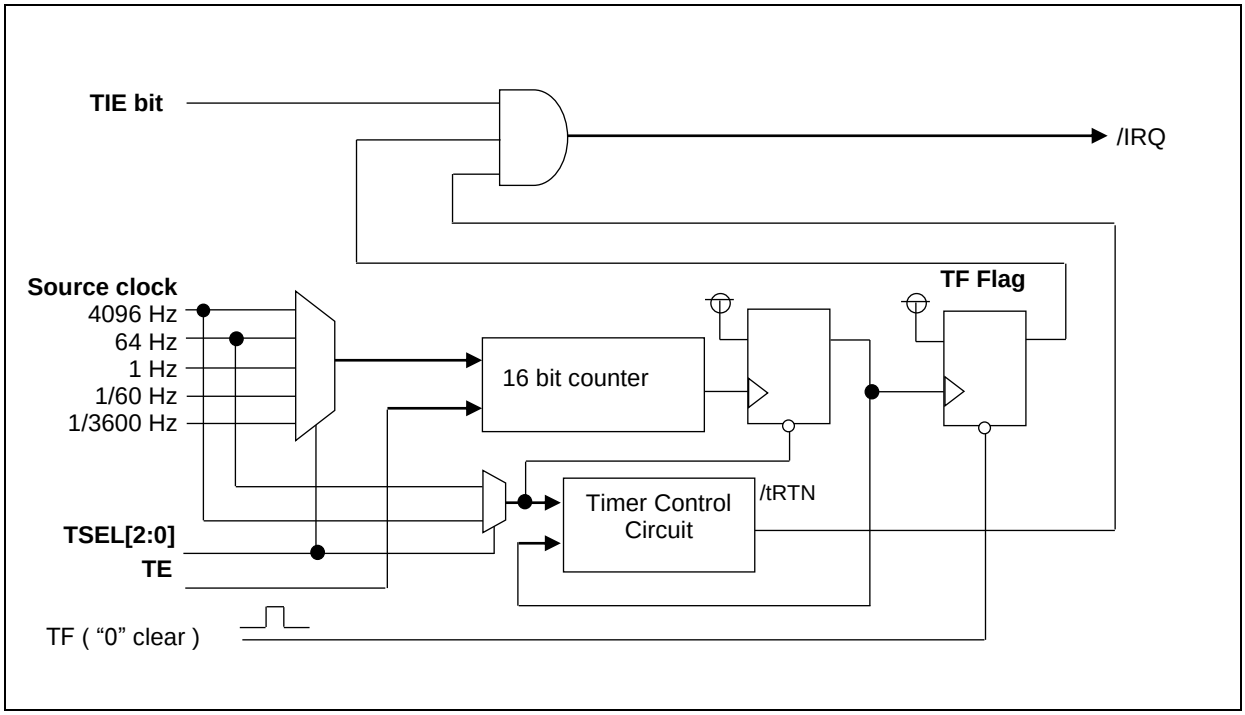


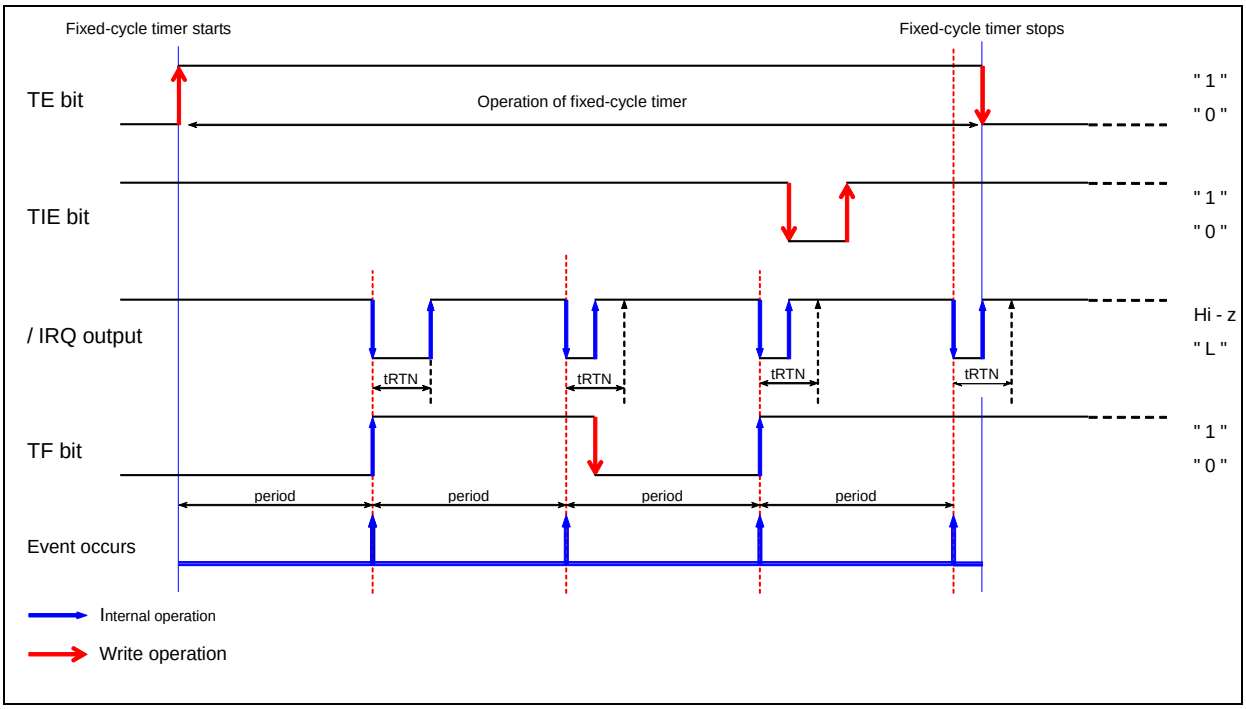
14.2.4. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings and fixed-cycle timer countdown setting sets interrupt interval, as shown in the following examples.

Timer Counter setting 1 ~ 65535	Source clock				
	4096 Hz TSEL2 = 0 TSEL1, 0 = 0, 0	64 Hz TSEL2 = 0 TSEL1, 0 = 0, 1	1 Hz TSEL2 = 0 TSEL1, 0 = 1, 0	1 / 60 Hz TSEL2 = 0 TSEL1, 0 = 1, 1	1 / 3600 Hz TSEL2 = 1 TSEL1, 0 = 0, 0
0	–	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min	1 h
:	:	:	:	:	:
410	100.10 ms	6.406 s	410 s	410 min	410 h
:	:	:	:	:	:
3840	0.9375 s	60.000 s	3840 s	3840 min	3840 h
:	:	:	:	:	:
4096	1.0000 s	64.000 s	4096 s	4096 min	4096 h
:	:	:	:	:	:
65535	15.9998 s	1023.984 s	65535 s	65535 min	65535 h

14.2.5. Diagram of fixed-cycle timer interrupt function





(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.

(2) When a time update interrupt event occurs, the UF bit value becomes "1".

(3) When the UF bit value is "1" its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /IRQ pin output is low if UIE = "1".
∗ If UIE = "0" when a timer update interrupt occurs, the /IRQ pin status remains Hi-Z.

(5) Each time an event occurs, /IRQ pin output is low only up to the tRTN time (which is fixed as min 7.57 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
∗ /IRQ pin output goes low again when the next interrupt event occurs.

(6) As long as /IRQ = low, the /IRQ pin status does not change, even if the UF bit value changes from "1" to "0".

(7) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

14.3. Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred. AF bit and /IRQ output show a maximum delay of 1.46ms from the alarm event.

∗ /IRQ="L" output when occurs alarm interruption event is not cancelled automatically unless giving intentional cancellation and /IRQ="L" is maintained.

14.3.1. Related registers for Alarm interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
17	MIN Alarm	**AE**	40	20	10	8	4	2	1
18	HOUR Alarm	**AE**	•	20	10	8	4	2	1
19	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1C	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	TSEL2	TSEL1	TSEL0
1D	Flag Register	VBLF	o	UF	TF	**AF**	RSF	VLF	VBFF
1E	Control Register0	***TEST***	STOP	UIE	TIE	**AIE**	TSTP	TBKON	TBKE

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg – 17h to 19h) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg – 17h to 19h) is being used as a RAM register, /IRQ may be changed to low level unintentionally.

1) Alarm registers

The minute, hour, day and date when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg – 19h), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.
Note: AE-bit is low active, so in order to enable 1 interrupt every hour once the actual minutes match the alarm setting, it is necessary to set the AE of register 17h to 0 and the AE of 18h and 19h to 1.
In order to generate an alarm interrupt only once a week, all 3 AE-bits have to be set "0

∗1) The alarm function is not a HW feature but software function inside the RTC!
*2) In case "AE" bit of register 19h is set to "1", the day will be ignored and an interrupt occurs ones the actual time matches the minutes and/or hour setting of the alarm register.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 19h):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only the hour and minute values match the alarm data.

∗3) If all three AE bit values are "1" the week/date and time settings are ignored and an alarm interrupt event will occur once per minute.

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-z) when an alarm interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)!
Read	0	–
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when an Alarm interrupt event has occurred.

AIE	Data	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

∗The AIE bit is only output control of the /IRQ terminal. It is necessary to clear an AF flag to cancel alarm.

14.3.2. Examples of alarm settings

1) Example of alarm settings when "Week" has been specified (and WADA bit = "0")

Week is specified WADA bit = "0"	Week Alarm								HOUR Alarm	MIN Alarm
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S		
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

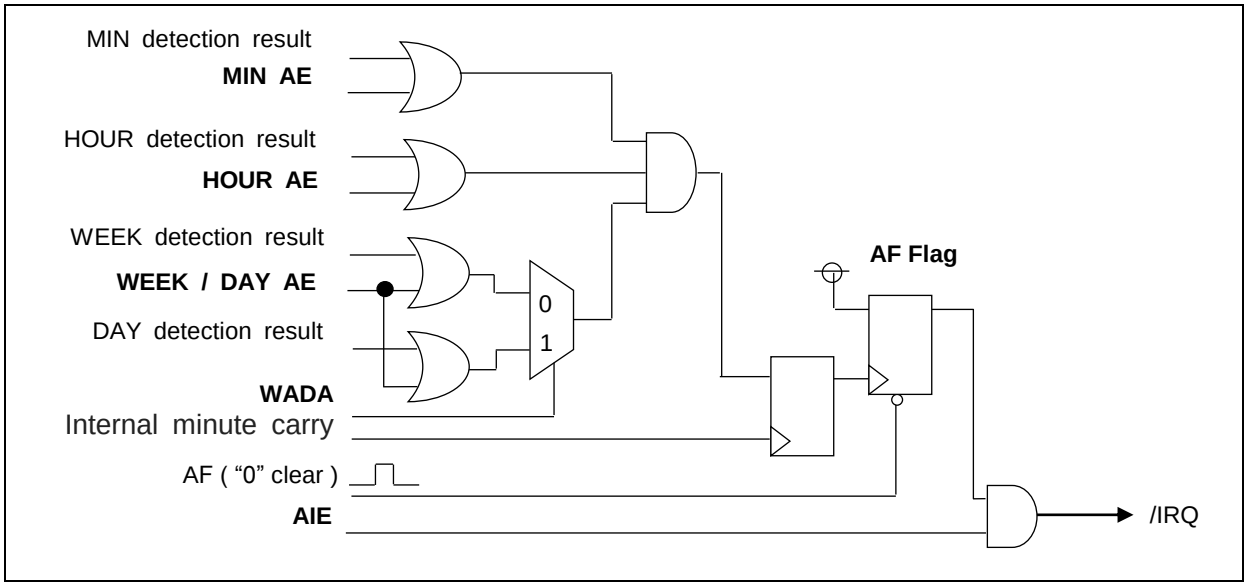
X: Don't care

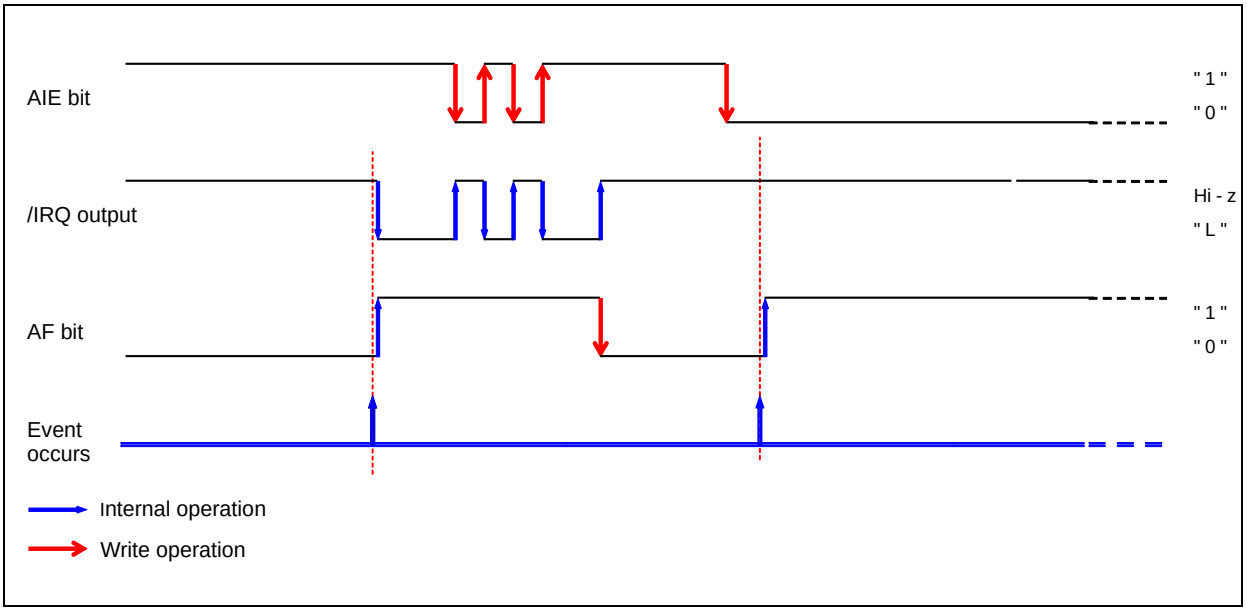
2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Day Alarm								HOUR Alarm	IN Alarm
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01		
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit = 1
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

14.3.3. Diagram of alarm interrupt function





14.4. Time Update Interrupt Function

The time update interrupt function generates interrupt in one-second or one-minute intervals which are synchronized to the update of the second or minute time register of the RTC When an interrupt event is generated, This /IRQ status is automatically cleared (/IRQ status changes from low level to Hi-z earliest 7.57ms (maximum 15.63ms) after the interrupt occurs).

14.4.1. Related registers for time update interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1C	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	TSEL2	TSEL1	TSEL0
1D	Flag Register	VBLF	o	**UF**	TF	AF	RSF	VLF	VBFF
1E	Control Register0	***TEST***	STOP	**UIE**	TIE	AIE	TSTP	TBKON	TBKE

∗ Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" time update interrupt events do not occur.

∗ Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

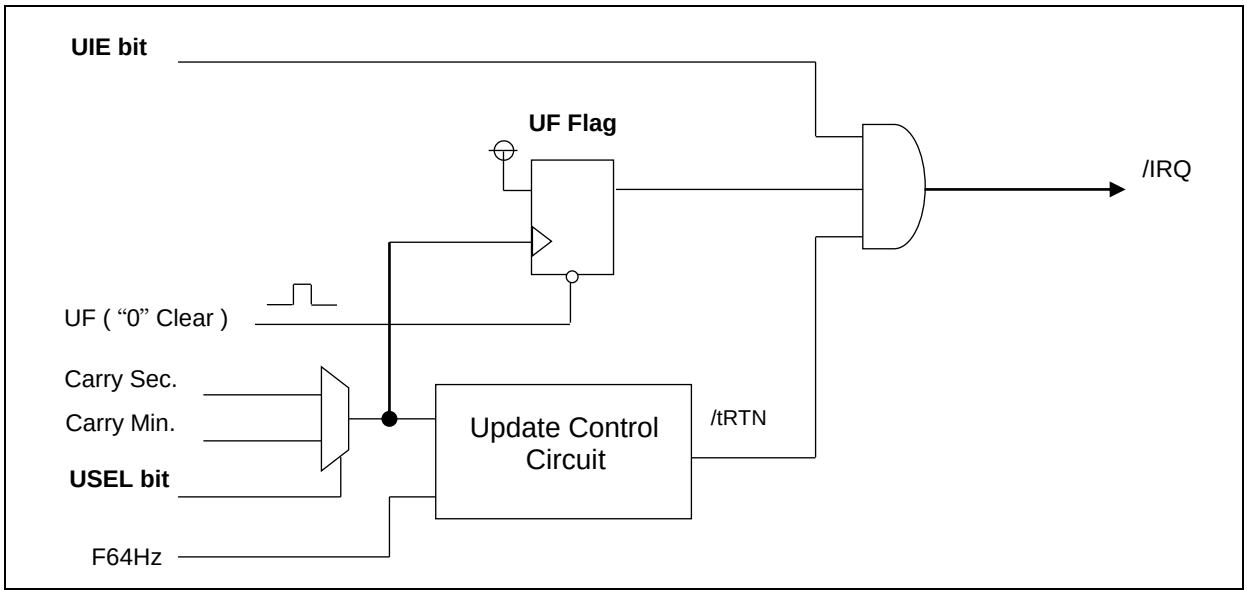
UF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-z) when an time update interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored
Read	0	–
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

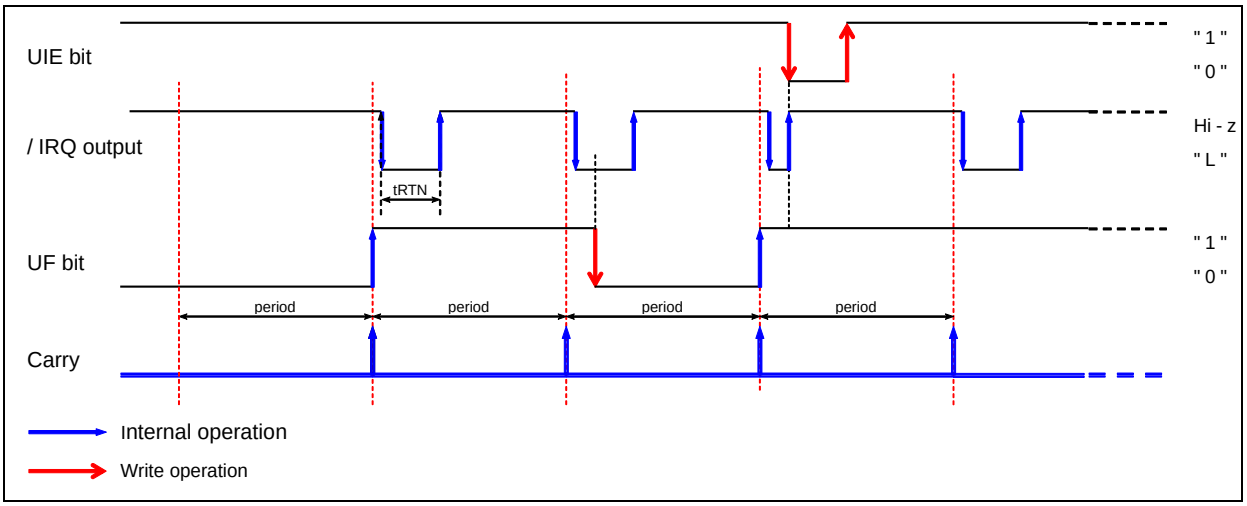
3) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs (/IRQ remains Hi-Z) 2) Cancels interrupt signal triggered by time update interrupt event (/IRQ changes from low to Hi-Z). ∗ Even when the UIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a time update interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). ∗ When a time update interrupt event occurs, low-level output from the /IRQ pin occurs only when the UIE bit value is "1". Earliest 7.57 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low to Hi-Z).

14.4.2. Time update interrupt function diagram





14.5. Frequency stop detection function

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss might have occureddue to supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.

14.5.1. Related registers for Frequency stop detection function and Voltage low detection function.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	○	UF	TF	AF	RSF	**VLF**	VBFF

1) VLF bit

VLF	Data	Description
Write	0	The VLF is cleared to 0, and waiting for next low voltage detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	RTC register data are valid.
	1	RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

14.6. FOUT function [clock output function]

The clock signal can be output via the FOUT pin. Output is stopped upon detection of the voltage drop below V_{DET1}In this case pin output becomes Hi-z.

14.6.1. FOUT control register.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1C	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	TSEL2	TSEL1	TSEL0

14.6.2. FOUT function table.

2) FSEL1,FSEL0 bit

FSEL1	FSEL0	output
0	0	32768 Hz Output
0	1	1024 Hz Output
1	0	1 Hz Output
1	1	OFF

X: don't care

∗ At the time of the initial power-on, "0" is set to FSEL1, FSEL0.

Note: The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz and 1024Hz output is possible.
But 1Hz output is disabled.

14.7. Battery backup switchover function

14.7.1. Description of Battery backup switchover function

It consists of the power-source detector "V_{DET}" which detect the power down of the main power source "V_{DD}", and built-in three MOS switches located between the main power-source pin "V_{DD}" and the backup power supply pin "V_{BAT}".
By switching three MOS switchs according to the result of the supply-voltage detection of V_{DET2}, the RTCs power supply is changed from V_{DD} to V_{BAT} (at the same time the RTC switches from normal to backup operation).
Thanks to the 3 MOS-switches, this power switching is performed without a reverse-current (from V_{BAT}->V_{DD}).
At the time VDD drops below VDET1 voltage (there are 2 options for VDET1, VDET11 and VDET12, which can be selected with RSVSEL-bit), the I/F-pins and FOUT-pin are deactivated (depenging on register settings) and a Reset-signal is output on the /RST-pin allowing to reset i.e. MCUs to avoid malfunction due to low supply voltage.
Until VDD drops below VDET2-voltage, the RTC will remain in normal operation mode and keep charging VBAT (depending on related register settings and conditions). Only if VDD drops below VDET2, the RTC will switch the power supply from VDD to VBAT.

14.7.2. Related register of Battery backup switchover function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	**VBLF**	○	UF	TF	AF	RSF	VLF	**VBFF**
1F	Control Register1	**SMP TSEL1**	**SMP TSEL0**	**CHG EN**	**INIEN**	○	RS VSEL	**BF VSEL1**	**BF VSEL0**

1) CHGEN bit

Charge ON/OFF control of backup battery.

CHGEN	Data	Description
Write / Read	0	MOS-Switches are OFF (defalt setting). Don't charge backup battery
	1	MOS-Switches are automatically controlled.

If INIEN-bit is set to "1", the RTC will automatically switch the power source, independent of the setting in CHGEN-bit.

2) INIEN bit

Control of MOS-Switch starts by setting "1" to this bit (at least once) and control of CHGEN is enabled.
Setting the INIEN-bit controls if the I/F-pins are kept active or are deactivated in the case the supply voltage on VDD drops below -V_{DET1}.
In order to enable control of the I / F, once it is necessary to set the INIEN bit to "1".

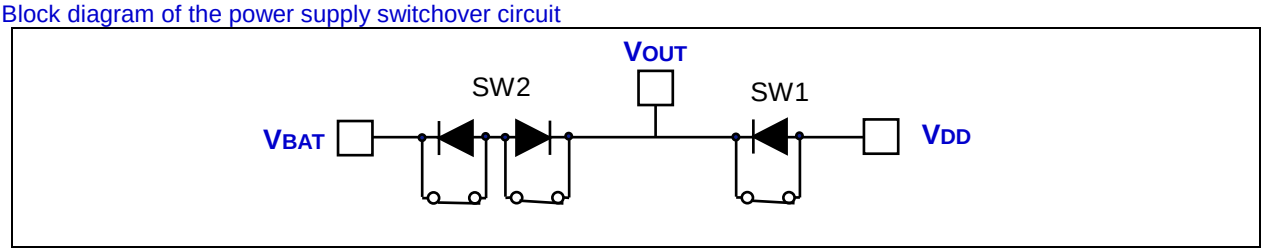
INIEN	Data	Description
Write / Read	0	If INIEN = 0 all time, CHGEN is ignored. In case INIEN was "1" once and even being set to "0" afterwards, CHGEN-bit remains valid and active
	1	CHGEN-bit is active and I/F is stopped upon detection of the voltage drop. Floating of a pin is permitted. Recommended setting.

3) State of MOS-Switch

A list of states

Scenarios	SW2	SW1	Description
A supply voltage is connected to V_{BAT} earlier than connected to V_{DD}.	OFF	OFF	The operation does not start until a supply voltage is applied to V_{DD}.
Initial power-ON by connecting supply voltage to V_{DD}.	OFF	ON	Backup power supply connected to VBAT is not charged until registers are set accordingly.
Primary cell (non rechargeable battery) connected to VBAT. .INIEN bit = 1, CHGEN =0	OFF	ON	V_{DD} operation
	ON	OFF	V_{DD}=OFF; backup operation from VBAT
A capacitor or a secondary battery (chargable) is connected to VBAT. INIEN bit = 1, CHGEN =1	ON	ON	V_{DD} operation and during battery charging.
	OFF	ON	V_{DD} operation and battery is charged fully. (Mode only enter if full charge detection is ON)
	ON	OFF	V_{DD}=OFF; backup operation from VBAT
A secondary battery (chargable) is connected to VBAT, and the full charge detection is OFF. INIEN bit = 1, CHGEN =1	ON	ON	V_{DD} operation and battery is always charged.
	ON	OFF	V_{DD}=OFF, backup operation from VBAT

Block diagram of the power supply switchover circuit



4) SMPTSEL1, SMPTSEL0 bit

V_{DD} voltage drop detection (V_{DET2}) constantly monitors the main supply voltage applied to VDD-pin and in case VDD drops below -VDET2 voltage, the power supply is switched from VDD to VBAT. For the monitoring of the VDD voltage, it is necessary to switch the MOS-switch SW1 (SW1 is located between the V_{DD}-V_{OUT}) off for the measurement time (to avoid measuring the voltage on VOUT-pin or supplied from VBAT).
Adjusting these bits allows to adopt the effective VDD Monitoring time to the discharge behavior on VDD and thus allow to make sure to grasp voltage drops safely.
Since VDET2 voltage detection is performed continuously and not only during the time SW1 is off, it is possible to detect VDD voltage drops under certain conditions at any time and not only when SW1 is off. To safely detect the VDD voltage drop, SW1 however has to be opened and SMPTSEL-registers need to be set carefully.
These registers do as well control the detection timing for the full charge detection (V_{DET3}) and Low-VBAT detection (V_{DET4}), which will control SW2.

Voltage detection (VDET1, VDET2, VDET3 and VDET4) times in different operation stages:

Power supply operation mode	SMPTSEL1,0	V_{DD} operation (Backup battery is charging)	V_{DD} operation (Backup battery is fully charged)	VDD operation (After return from backup V_{DET1}>V_{DD}>V_{DET2})
SW1 Off time. *	00b (default)	2ms	2ms	2ms
	01b	16ms	16ms	2ms
	10b	128ms	128ms	2ms
	11b	256ms	256ms	2ms

* Time values in above list are only for reference.

Operation stages of voltage detection:

Power supply operation mode	VDD operation (Backup battery is charging)	VDD operation (Backup battery is fully charged)	VDD operation (After return from backup V_{DET1}>V_{DD}>V_{DET2})	VBAT operation (Backup mode)
Reset & I/F stop threshold detection V_{DET1}	Constantly ON	Constantly ON	Constantly ON	Constantly OFF
Power switching detection V_{DET2}	Constantly ON	Constantly ON	Constantly ON	Once/31.25ms
Full charge detection V_{DET3}	Once/1.0s	Once/1.0s	Once/1.0s	Constantly OFF
Low-VBAT detection V_{DET4}	Once/1.0s	Once/1.0s	Once/1.0s	Constantly OFF

* In V_{DD} operation the MOS-switch 1 has to be opened (Off) to detect the VDD voltage supply. Above mentioned times for VDD monitoring correspond to this MOS-switch Off (opening) times.

5) BFVSEL1, BFVSEL0 bit

Setting the full charge detection threshold voltage to stop charging of the backup battery.

BFVSEL1	BFVSEL0	Description
0	0	3.02 V (default)
0	1	3.08 V
1	0	2.92 V
1	1	OFF (Don't stop charge)

The full-charge detection (V_{DET3}) and over-discharge detection (V_{DET4}) control SW2.

6) VBFF bit

VBFF	Data	Description
Read	0	–
	1	Full charge of VBAT detected (voltage level defined by BFVSEL-bit is reached)

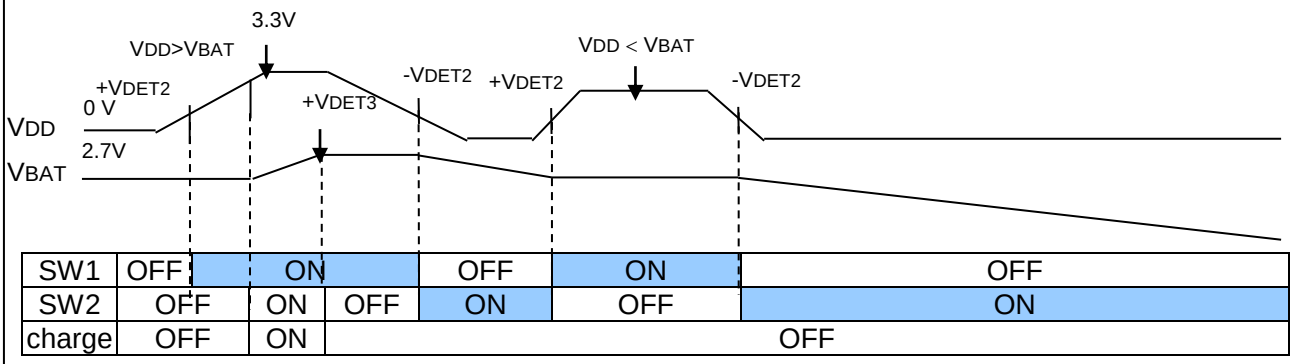
This flag shows a charge state.

7) VBLF bit

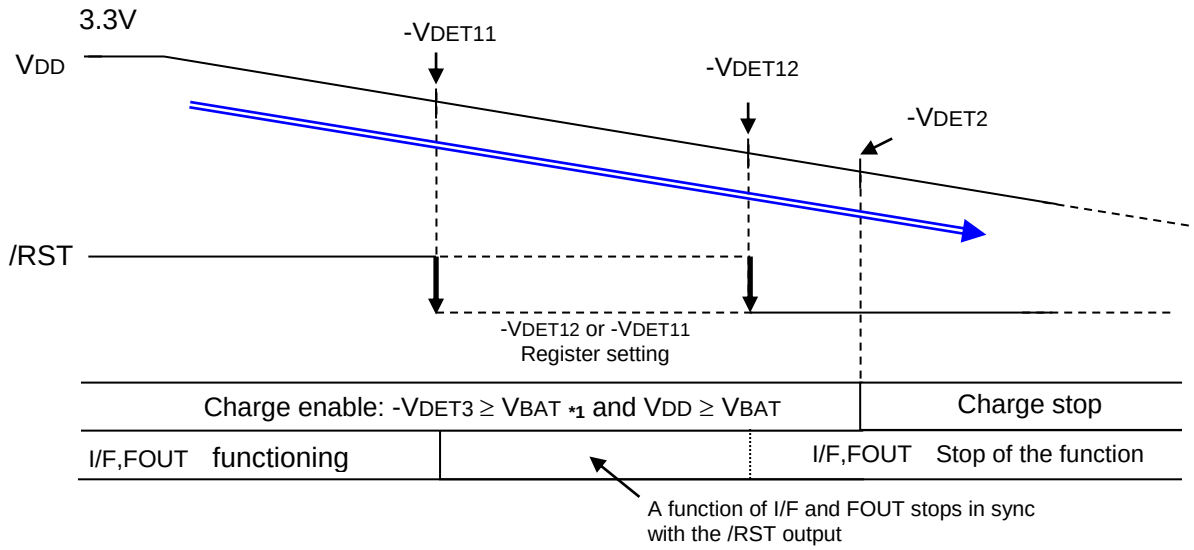
VBLF	Data	Description
Write	0	Cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	–
	1	Low-VBAT has been detected (VDET4)

14.7.3. Power supply control outline

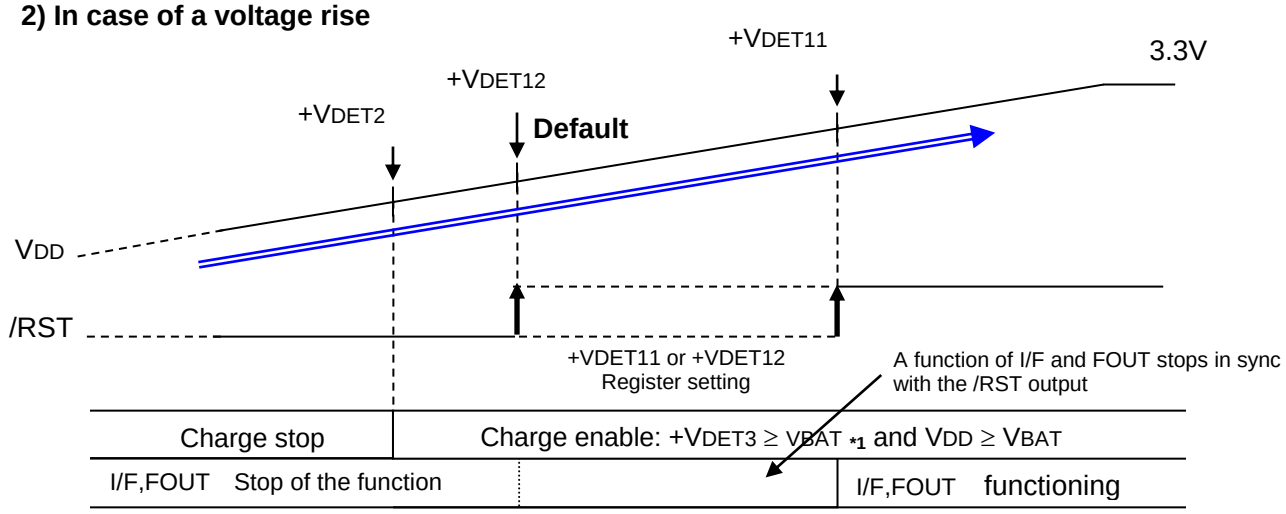
Timing chart of switch control and battery charging



Main power supply (V_{DD}) voltage and operation state



2) In case of a voltage rise

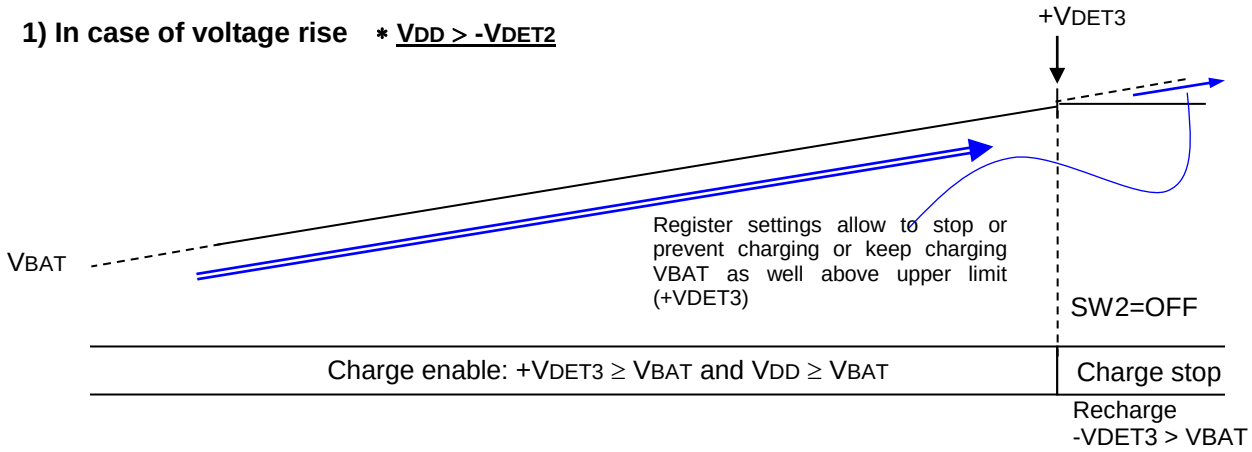


*1 When full charge detection was deactivated (VDET3) by register setting, VBAT is only charged if VDD > VBAT

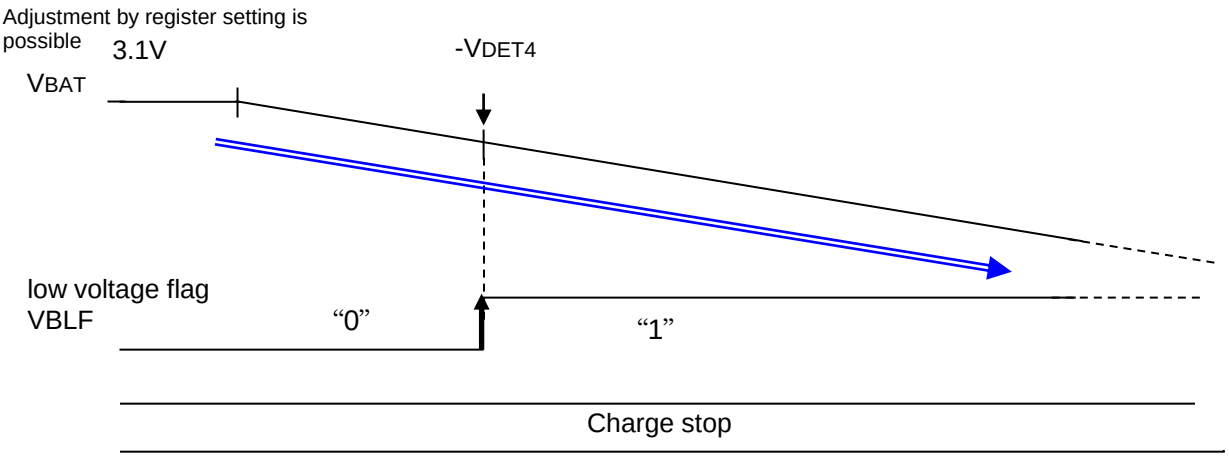
Backup power supply (V_{BAT}) voltage and a charge state

Adjustment by register setting is possible

1) In case of voltage rise * **$V_{DD} > -V_{DET2}$**



2) In case of voltage drop * **$V_{DD} \leq +V_{DET2}$**



14.8. Reset output function

This RTC has a built-in Reset-Controller, which outputs a Reset-signal on the /RST-pin to control external HW like MCUs in case of a drop in supply voltage. When the V_{DD} voltage drops below VDET1 (register selectable VDET11 or VDET12), a /RST-signal is output. Once VDD raises beyond VDET1 voltage again, the /RST-signal is released.
In case INIEN bit is set to "1", I/F and FOUT are stopped when VDD drops below VDET1.

14.8.1. Related register of reset output function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	o	UF	TF	AF	**RSF**	VLF	VBFF
1F	Control Register1	SMP TSEL1	SMP TSEL0	CHG EN	INIEN	o	**RS VSEL**	BF VSEL1	BF VSEL0

1) RSVSEL-bit

Setting of VDET1 voltage level. In case VDD dropps below this level, the /RST-signal is output and the I/F and FOUT output are stopped (depending on INIEN-bit setting).

RSVSEL	Data	Description
Write / Read	0	$-V_{DET11}$ (2.75V) (default)
	1	$-V_{DET12}$ (2.7V)

2) RSF-bit

This bit holds the result of detecting the reset voltage.

RSF	Data	Description
Write	0	The RSF is cleared to 0, and waiting for next low voltage detection.
	1	Invalid (writing a 1 will be ignored)
Read	0	-
	1	A voltage drop below -VDET1 was detected.

14.9. Detection voltage setting

Overview of detection voltage levels

	Item	Symbol	Detect voltage(Typ)	setting
V_{DET1}	Reset /Reset-release voltage	$+V_{DET11}$ / $-V_{DET11}$	2.8V / 2.75V	RSVSEL “0” (default)
		$+V_{DET12}$ / $-V_{DET12}$	2.7V / 2.65V	RSVSEL “1”
V_{DET2}	Backup switchover/recover voltage	$+V_{DET2}$ / $-V_{DET2}$	1.35V / 1.30V	
V_{DET3}	Full charge detection voltage	$+V_{DET31}$ / $-V_{DET31}$	3.02V / 2.97V	BFVSEL “00b”(default)
		$+V_{DET30}$ / $-V_{DET30}$	2.92V / 2.87V	BFVSEL “01b”
		$+V_{DET32}$ / $-V_{DET32}$	3.08V / 3.03V	BFVSEL “10b”
V_{DET4}	VBAT low-voltage detection voltage	$-V_{DET4}$	2.4V	

14.10. Digital offset function

With this function it is possible to increase or decrease the speed of the time counting and thus put an positive or negative offset to the clock precision. The adjustment range for this offset correction is $+192.3\times10^{-6}$ to -195.3×10^{-6} in steps of 3.05×10^{-6}.

14.10.1.Digital offset register

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1

- DTE=”1” enables the digital offset function.

When the digital offset function is enabled, the digital offset register digitally offsets the sub-second clocks according to the values set in the digital offset register. This correction of the second time register occurs every 10 seconds and the level of correction depends on the offset required. When outputting a 32.768kHz signal on FOUT-pin , this function has no influence, since the oscillation frequency of the built-in crystal does not change by using this function. In case of outputting a 1Hz or 1024Hz signal on FOUT, the offset correction will cause a certain jitter on the clock signal.
Alarm function as well as the Fixed Cycle Timer function (if source clock lower than 4kHz is selected) are affected by this function.

- In order to disable the digital offset function, set to DTE = ”0”. In this case the L1 to L7 are ignored.

- Below table shows the relationship of the L7~L1 bit and the digital offset value

When the L7 bit = “0”, the offset is positive (clock runs faster), when the L7 bit = “1”, the offset is negative (the clock runs slower).

Digital offset bits							Offset value
L7	L6	L5	L4	L3	L2	L1	($\times 10^{-6}$)
0	1	1	1	1	1	1	+192.26
0	1	1	1	1	1	0	+189.21
			• •				• •
0	0	0	0	0	1	0	+6.10
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0.00
1	1	1	1	1	1	1	−3.05
1	1	1	1	1	1	0	−6.10
			• •				• •
1	0	0	0	0	0	1	−192.26
1	0	0	0	0	0	0	−195.31

The offset value are calculated on basis of a shift of the built-in crystal frequency.

- How to calculate the offset value

1) When the offset value is positive:

L [7 ~ 1] =[Offset Value]/ 3.05 However, decimals are discarded.

Example calculation: When the offset value is +192 × 10^{-6}

L[7 ~ 1] = 192.26 / 3.05 = 63 (dec)

= 0111111(bin) is set.

2) When the offset value is negative:

L[7 ~ 1] = 128 – [Offset Value] / 3.05 However, decimals are discarded.

Example calculation: When the offset value is –158 × 10^{-6}

L[7 ~ 1] = 128 - (158 / 3.05) = 76(dec)

= 1001100(bin) is set.

3) When calculate from accuracy of a clock

To adjust 30 seconds in 30 days:

Example calculation: 30sec. / 2592000s (30days) = 11.57 × 10^{-6}

Positive offset

L[7 ~ 1] = 11.57 / 3.05 = 4 (dec) However, decimals are discarded.

= 0000100(bin) is set.

Negative offset

L[7 ~ 1] = 128 – (11.57 / 3.05) = 124 (dec) However, decimals are discarded.

= 1111100(bin) is set.

14.10.2. Effect of the digital offset function to other functions

Because this function adjusts an internal sub-second clock, this function affects the a Fixed-cycle timer interrupt function and FOUT function

1) FOUT funtion

- 1Hz setting: Once in 10 seconds, the 1Hz period fluctuates.
- 1024Hz setting: Once in 10 seconds, the 1024Hz period fluctuates.

∗There are cases where there is no fluctuation, depending on the offset correction value..

- 32.768kHz Not affected.

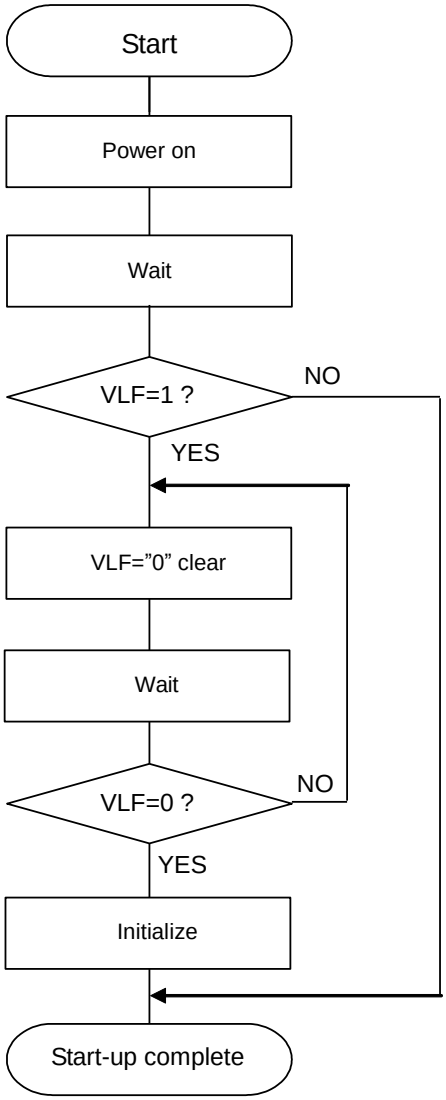
2) Fixed-cycle timer interrupt function

- 64Hz or 1Hz source clock setting: Once in 10 seconds, the period fluctuates.
  When the timer intervals are long, the fluctuations appear small.
- 4kHz source clock setting: Not affected.

14.11. Flow-chart

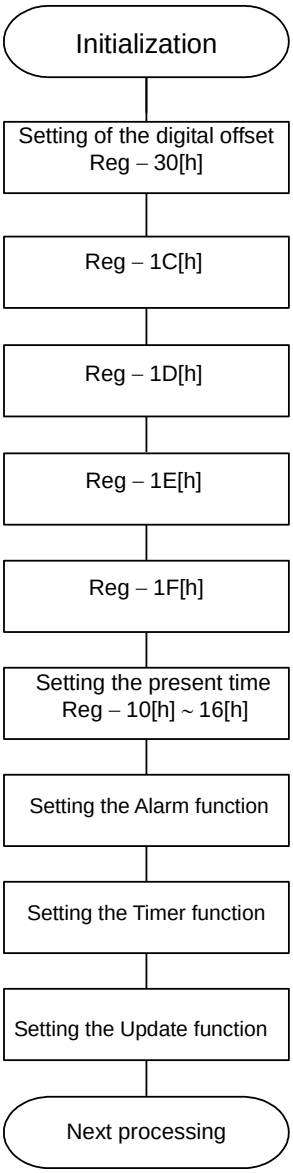
The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

1) Processing example at the time of power-on, after internal oscillation stabilized (VLF stays “0”)



- Wait time of 30 ms is necessary at least.
  Wait time of 35 ms or more is necessary when returning from backup.
- Whether it is a return from the state of the backup is confirmed.
- When an internal oscillation starts, 0 writing of VLF is approved.
- Please set waiting time depending on load of a system optionally.
  It takes about 200 ms from Power ON to oscillation start.

2) Example of Initialization routine



- When the digital offset function is not being used, write 0 in the DTE bit.

- Set TE bit to “0”.
- Set FSEL1, 0 bit optionally.

- Clear VLF bit to “0”.
  State of VLF=1 is held even if it 0 clear until oscillation start. When initialize it without waiting for an oscillation start, Clear VLF bit after an oscillation start.
- Set the Battery backup switchover function.
  In a default state, charge to V_{BAT} does not start it.

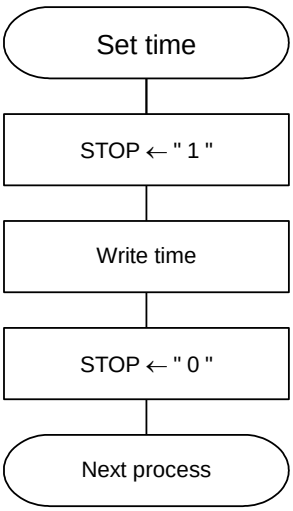
- Surely set TEST bit to " 0 ".
- Set AIE, TIE, UIE bit to “0 " to prevent unprepared interruption output.

- Set the present time.
  ∗ Setting the present time concerned, please refer to item of [Clock and calendar writing] .

- Set the Alarm interrupt function.
  When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
- Set the fixed-cycle Timer function.
  When the fixed-cycle timer function is not being used, the Timer Counter register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.
- Set the Update interrupt function.

∗ When initialization is finished, be sure to set STOP bit to “0”.

3) The setting of the clock and calendar



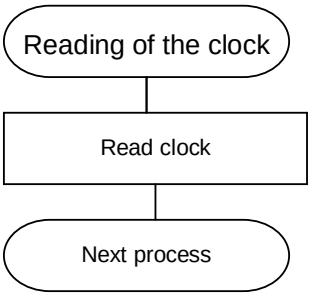
- Set STOP bit to “1” to prevent timer update in time setting.

- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset).
  In case of initialization, please initialize all data.

- Cancel STOP bit to “0” and start (restart) timer movement.
  Timer is started when set STOP bit to “0”.

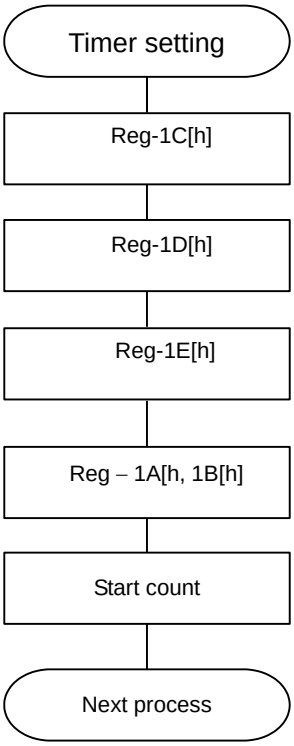
∗ It is able to set time even if not combined use of STOP bit.
Please note that [clock is started at the time of writing [second]] in case STOP bit is not used. When STOP = 1, please be aware that the functions such as the voltage detection function stop.

4) The reading of the clock and calendar



- Please complete access within 0.95 seconds
  The STOP bit holds "0".
  (It causes the clock delay to set STOP bit to “1”)
- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.
- The access to a clock calendar recommends to have access to continuation by a auto increment function.

5) Setting example of the fixed-cycle timer interrupt function



- Clear TE bit to “0” to stop timer-interrupt function.
- The countdown period is fixed by the combination of the TSEL2, TSEL1, TSEL0 bit.

- Clear TF bit to “0” to cancel last timer interrupt output (/IRQ output).

- Select and set /IRQ output
- Select a power supply condition of a count

- Set initial value of down counter.

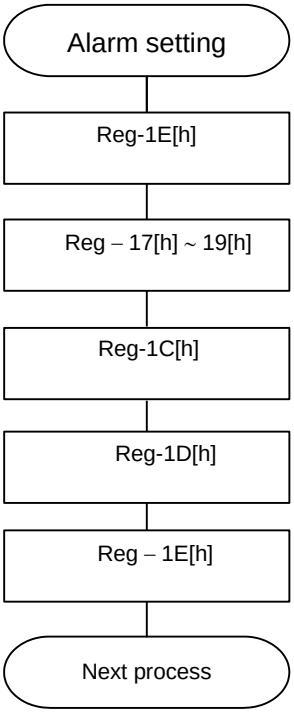
- Set TE bit to "1" to start timer interrupt function.

When start timers interrupt function, please surely set/reset (*implement 2) initial value of down counter in advance.

∗1 Countdown is suspended with TSTP, " 0 " → " 1 " and countdown is performed again with TSTP, " 1 " → " 0 "

∗2 When you want to restart from a pre-set value, please set a TE bit to “1” again after setting a TE bit to “0”.

6) Setting example of the Alarm interrupt function



- Set AIE bit to “0” to stop Alarm-interrupt function.
- Set alarm data.
- Select week or day in WADA bit
- Clear AF bit
- Select and set /IRQ1 output in AIE bit.

14.12. Reading/Writing Data via the I²C Bus Interface

14.12.1. Overview of I²C-BUS

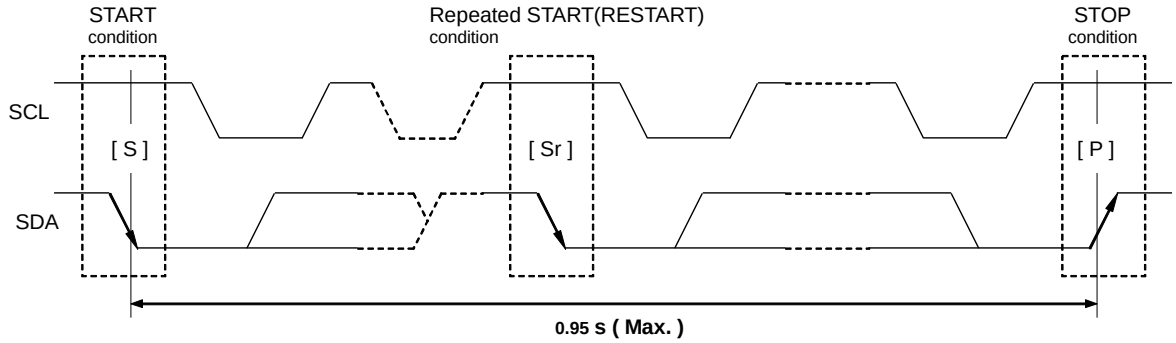
The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

14.12.2. Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.95 seconds.)

14.12.3. Starting and stopping I²C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition
- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition
- This condition regulates how communications on the I²C -BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)

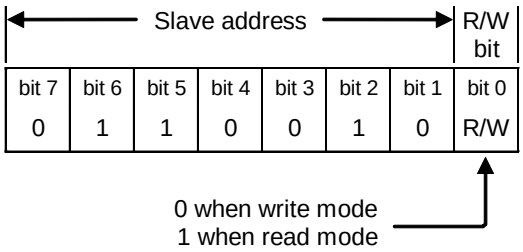
- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

- When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds.If communication requires 0.95 seconds or longer, the I²C bus interface is reset by the internal bus timeout function.

14.12.4. Slave address

The I²C-BUS devices do not have any chip select or chip enable pins. All I²C-BUS devices are memorized with a fixed unique number in it. The chip selection on the I²C-BUS is executed, when the interface starts, the master device send the required slave address to all devices on the I²C-BUS. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.

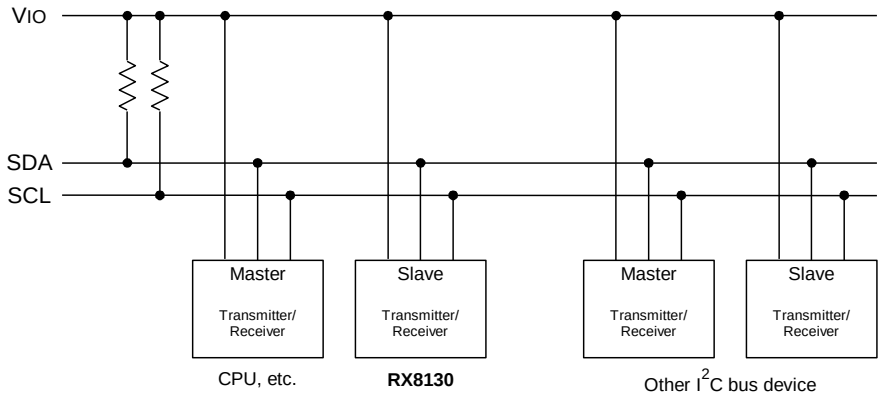
During in actual data transmission, the transmitted data contains the slave address and the data with R/W (read/write) bit.



14.12.5. System configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VIO line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

14.12.6. I²C bus protocol

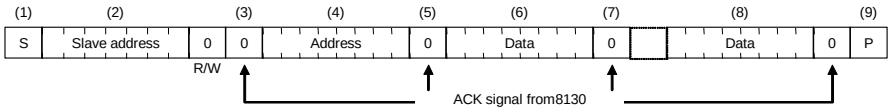
In the following sequence descriptions, it is assumed that the CPU is the master and the RX8130 is the slave.

1) Address specification write sequence

Since the RX8130 includes an address auto increment function, once the initial address has been specified, the RX8130 increments (by one byte) the receive address each time data is transferred.

Address circulation of auto increment function.	10[h] ->1F[h] -> 10[h]
	20[h] ->2F[h] -> 20[h]
	30[h] ->3F[h] -> 30[h]

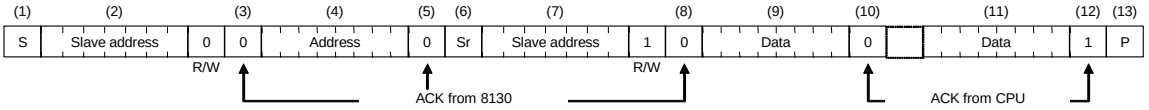
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8130's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8130.
(4) CPU transmits write address to RX8130.
(5) Check for ACK signal from RX8130.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX8130.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



2) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

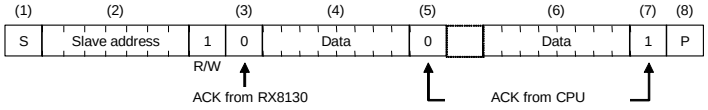
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8130's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8130.
(4) CPU transfers address for reading from RX8130.
(5) Check for ACK signal from RX8130.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX8130's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX8130 (from this point on, the CPU is the receiver and the RX8130 is the transmitter).
(9) Data from address specified at (4) above is output by the RX8130.
(10) CPU transfers ACK signal to RX8130.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].



3) Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8130's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX8130 (from this point on, the CPU is the receiver and the RX8130 is the transmitter).
(4) Data is output from the RX8130 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX8130.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX8130.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].



Application Manual

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